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Design and Evaluation of an L-Band Current-Mode Class-D Power Amplifier Integrated Circuit

Michael J. Shusta
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Design and Evaluation of an L-Band Current-Mode Class-D Power Amplifier Integrated Circuit

A Thesis Presented

by

MICHAEL J. SHUSTA

Submitted to the Graduate School of the University of Massachusetts Amherst in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL AND COMPUTER ENGINEERING

May 2014

Electrical and Computer Engineering
Design and Evaluation of an L-Band Current-Mode Class-D Power Amplifier Integrated Circuit

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MICHAEL J. SHUSTA

Approved as to style and content by:

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Robert W. Jackson, Chair

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Joseph Bardin, Member

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Christopher Salthouse, Member

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C. V. Hollot, Department Head
Electrical and Computer Engineering
DEDICATION

For my parents:

For my father, who taught me commitment at a young age.
For my mother, who focused that commitment on education.
These are the sort who raise excited students.
ACKNOWLEDGEMENTS

I would first like to thank my advisor, Professor Robert Jackson, for his patience in guiding my graduate study at UMass – he was even kind enough to teach electronics to me as an undergraduate here. Professors Joseph Bardin and Christopher Salthouse deserve thanks for many productive conversations related to this work, in addition to sitting on the thesis committee.

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A thank you to colleagues who have been a source of both humor and wisdom throughout this project is in order – namely to Ajay Subramanian and Martin Muthee. I would also like to extend my gratitude to Hossein Nemati, who shared with me an insightful copy of his prior work. Finally, I would like to extend a belated thank you to Professor Paul Siqueira, Harish Vedantham, and Razi Ahmed, who had a profound effect on my professional trajectory since I was their undergraduate assistant in the field of remote sensing. These three introduced me to microwave engineering, which I would study over the next six or so years. In that time I benefited greatly from the microwave culture at UMass, due in no small part to people like Professors Jackson, Siqueira, and Janaswamy to name only the few I learned most from.
ABSTRACT

DESIGN AND EVALUATION OF AN L-BAND CURRENT-MODE CLASS-D POWER AMPLIFIER INTEGRATED CIRCUIT

MAY 2014

MICHAEL J. SHUSTA, B.S., UNIVERSITY OF MASSACHUSETTS AMHERST
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Directed by: Professor Robert W. Jackson

Power amplifiers (PAs) convert energy from DC to high frequencies in all radio and microwave transmitter systems be they wireless base stations, handsets, radars, heaters, and so on. PAs are the dominant consumers of energy in these systems and, therefore, the dominant sources of system cost and inefficiency. Research has focused on efficient solid-state PA circuit topologies and their optimization since the 1960s. The 2000s saw the current-mode class-D (CMCD) topology, potentially suitable for today's wireless communications systems, show promise in the UHF frequency band. This thesis describes the design and testing of a high-efficiency CMCD amplifier with an integrated driver stage. In addition, analysis of a merged PA-mixer circuit based on the CMCD is provided.
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CHAPTER 1
INTRODUCTION

Power amplifiers (PAs) convert energy from DC to high frequencies in all radio and microwave transmitter systems be they wireless base stations, handsets, radars, heaters, and so on. PAs are the dominant consumers of energy in these systems and, therefore, the dominant sources of system cost and inefficiency [1,2,3]. Research has focused on efficient solid-state PA circuit topologies and their optimization since the 1960s [4]. The 2000s saw the current-mode class-D (CMCD) topology, potentially suitable for today's wireless communications systems, show promise in the UHF frequency band. This thesis describes the design and testing of a high-efficiency CMCD amplifier with an integrated driver stage. In addition, an investigation of the CMCD within a merged PA-mixer circuit is provided. This chapter details the CMCD circuit, reviews similar work and related PA topologies, and presents the goals of this thesis.

1.1 Current-Mode Class-D Power Amplifier Theory

The appeal of the current-mode class-D power amplifier is best understood via a brief overview of power amplifier taxonomy [5]. Traditional PAs, shown schematically in Appendix A to this thesis, operate with the active device in a linear mode. These PA classes, 'A' and 'B', differ in their nominal conduction angles – the portion of the RF (radio-frequency) cycle in which the active device conducts current. In class-A operation, a full cycle of conduction provides the most linear but least efficient option – that is, the
least output power per absorbed DC and drive power of all amplifier classes. In class-B operation the device conducts for half of the cycle, typically appearing in a symmetric, 'push-pull' configuration trading the load current with another device. This prevents the two devices from dissipating power in the half-cycle in which they are cut off, just as the voltages they sustain at their outputs are greatest. Thus, efficiency is improved with respect to class-A designs: class-B provides 78.5% maximum theoretical efficiency, while class-A provides 50%.

Further reduction of the conduction angle below a half-cycle, class-C operation, provides additional efficiency at the cost of achievable output power and linearity. A tuned circuit to filter harmonic distortion at the load is a necessity in this scenario (as well as in class-B applications). The maximum theoretical efficiency of the class-C topology approaches 100% as the conduction angle and output power go to zero [5]. However, the output power at a given conduction angle may be increased by driving the active device with more power, such that the class-C amplifier becomes 'saturated', the device's response becoming more non-linear. Moving further into the non-linear and high-efficiency regime the designer arrives at classes D through F: the switchmode power amplifiers (SMPAs) currently under study for use in today's wireless systems.¹

Switchmode, or 'switching', topologies employ the active device, or devices, with enough drive to force two on/off switching states, cut-off and triode (linear resistance) in the case of a field-effect device, analogous to a switch with finite on-state resistance and

---

¹ Traditional class-D (voltage-mode class-D), class-E, and traditional class-F are not discussed in detail in this thesis. The interested reader is directed to references 4, 5, 6, 7, 8 and 9.
infinite off-state resistance [6]. These two operating regions are highlighted in Figure 1.1. In SMPAs, a tuning network between the device and the load 'shapes' the non-linear circuit response at the device's output terminals while filtering out the harmonic content flowing to the load, seen in the simplified block diagram of a switching PA in Figure 1.2. This 'waveshaping' network, often referred to as a 'harmonic termination' or 'harmonic tuning' network is designed to translate the load impedance at the fundamental design frequency to the device's optimum while providing a combination of open and short-circuit load conditions to the device at higher harmonics of the operating frequency\(^2\). This allows one to minimize concurrent voltage and current swing – that is, power dissipation in the device – at each harmonic since either little to no current flows into the network (open harmonic load) or little to no voltage develops across the network (short harmonic load) when forced by the non-linear switch at its input. Thus, one may eliminate most power dissipation in the RF cycle by controlling the harmonic content of the phenomena at the switch, or switches, while filtering those features at the load, thereby giving an undistorted output to realize efficiencies in excess of class-B without the diminished output power of class-C.

\(^2\) The class-E SMPA stands alone in this regard: its load network is designed with time-domain considerations [7].
The current-mode class-D topology, an overdriven form of push-pull class-B with the two switching devices conducting square current pulses in antiphase, and the inverse class-F topology, in which a single device generates current harmonics shaped to square pulses with half-wave sinusoidal voltage response, have distinct advantages in their ability to absorb the capacitive parasitics of switching devices into the termination network in order to maintain high efficiency at higher frequencies. The CMCD, two forms of which are shown schematically in Figure 1.3, is in fact a push-pull version of the inverse class-F topology, where its balanced structure provides much of the required harmonic terminations rather than a complex distributed network. It provides a
maximum theoretical efficiency of 100%. In these ways, the current-mode class-D PA allows designers to combat some of today's major wireless challenges: DC power and cooling costs of infrastructure, limited handset battery life, and outsize form factors [1,2,3,4]. Sections 1.1.1 and 1.1.2 of this chapter describe the operation of the basic CMCD topologies, while section 1.1.3 covers briefly the inverse-F PA.

![Figure 1.3](image)

**Figure 1.3** The transformer-coupled (left) and symmetric (right) current-mode class-D RF power amplifier topologies.

### 1.1.1 The Transformer-Coupled CMCD Amplifier

The *transformer-coupled* current-mode class-D amplifier, displayed with relevant details in Figure 1.4, relies on the balanced structure of a push-pull amplifier and the parallel, tuned resonator, or 'tank', before the load to satisfy its terminating criteria: short-circuit terminations at the odd harmonics of the operating frequency, and open-circuit terminations at the even harmonics\(^3\). The circuit should first be understood in

\(^3\) In this thesis, 'odd' and 'odd-order' are used interchangeably to refer to harmonics of some example frequency \(\omega\) at \(3\omega\), \(5\omega\), \(7\omega\) and so on. Likewise, 'even' and 'even-order' refer to frequencies \(2\omega\), \(4\omega\), \(6\omega\), etc.
principle before discussing particularly how these criteria are achieved [5].

![Detailed transformer-coupled CMCD schematic.](image1)

**Figure 1.4** Detailed transformer-coupled CMCD schematic.

![Drain-source current and voltage waveforms of transformer-coupled CMCD devices.](image2)

**Figure 1.5** Drain-source current and voltage waveforms of transformer-coupled CMCD devices.

First, it is seen that a choke inductor feeds DC current into the center-tap of the balun transformer on the primary side. The two switching devices are driven by
complementary signals at some frequency $\omega_{RF}$ assumed to have sufficient swing in order to place the devices instantaneously in the on and off positions described in the prior section. Therefore, the DC current is steered back and forth between the two switches, each for a half-cycle, resulting in square current waveforms $i_1(t)$ and $i_2(t)$ with fundamental frequency $\omega_{RF}$ as seen in Figure 1.5. Taking the turns ratio from each primary to the single-ended secondary as $m:n$, these currents reflect across the transformer balun toward the load to take the form:

$$i_3(t) = \frac{4}{\pi} \frac{m}{n} I_{dc} \sum_{k=0}^{\infty} \sin((2k+1)\omega_{RF} t)$$

The resonator comprised of inductor $L_0$ and capacitor $C_0$ is designed to resonate at $\omega_{RF}$ with sufficient quality factor to ensure that all frequency components of current $i_3(t)$ beyond the fundamental are shunted to ground such that the load current and voltage are:

$$i_L(t) = \frac{4}{\pi} \frac{m}{n} I_{dc} \sin(\omega_{RF} t), \quad v_L(t) = \frac{4}{\pi} \frac{m}{n} I_{dc} R_L \sin(\omega_{RF} t)$$

Reflecting this load voltage across the transformer to the primary side dictates the following voltage between the drains of the two devices:

$$v_{ds_1}(t) - v_{ds_2}(t) = \frac{8}{\pi} \left( \frac{m}{n} \right)^2 I_{dc} R_L \sin(\omega_{RF} t)$$

However, for each half-cycle the devices are alternately near shorts to ground while they are switched on. Assuming that they present no resistance to ground for this simplified analysis, the half-sinusoidal drain-source waveforms of Figure 1.5 result: each switch
sustains a half-cycle of the swing across the primary windings while the opposing switch holds the opposite balun terminal at ground. The current and voltage waveforms show no overlap. No power has been lost in the switches, yet RF power has been converted from DC and fed to the load, illustrating 100% efficiency. It is clear that the transformer center-tap and the switch drain-source voltages must have DC value $V_{DD}$. From Fourier analysis, the drain-source waveform of the switches is:

$$V_{ds_1}(t) = V_{DD} + \frac{\pi}{2} V_{DD} \sin(\omega_{RF} t) - V_{DD} \sum_{k=1}^{\infty} \frac{2}{(2k)^2 - 1} \cos(2k \omega_{RF} t)$$

$$V_{ds_2}(t) = V_{DD} - \frac{\pi}{2} V_{DD} \sin(\omega_{RF} t) - V_{DD} \sum_{k=1}^{\infty} \frac{2}{(2k)^2 - 1} \cos(2k \omega_{RF} t)$$

implying that the load voltage has peak $\pi V_{DD} \left(\frac{n}{2m}\right)$ giving RF output power:

$$P_L = \frac{(\pi \frac{n}{2m} V_{DD})^2}{\frac{2}{2 R_L}} = \frac{\pi^2 V_{DD}^2}{8 \left(\frac{m}{n}\right)^2 R_L}$$

and the DC current demanded by the circuit in terms of other constants:

$$|v_L(t)| = \frac{4}{\pi n} m I_{dc} R_L = \pi V_{DD} \left(\frac{n}{2m}\right) \Rightarrow I_{dc} = \frac{\pi^2 V_{DD}}{8 \left(\frac{m}{n}\right)^2 R_L}$$

where it can be seen that the output power and DC power absorbed by the circuit are equal.

To understand the CMCD from a harmonic tuning perspective, it should be reiterated that the square currents flowing through the switches are comprised of a DC component, a fundamental component, and odd harmonics, while the half-wave
sinusoidal voltages across the switches consist of a DC portion, the fundamental, and even-order harmonic components: the intervening network between the switches and the single-ended load has shaped these waveforms appropriately to eliminate cross-over between the current and voltage. The transformer balun connecting the transistors enforces an open-circuit condition at all even multiples of the fundamental frequency.

This is best understood with a fresh example: consider the two switches as identical, non-linear transconductances driving a balanced load as in Figure 1.6, which might generate short-circuit currents at higher harmonics according to:

\[
i_{ds_{1,2}}(t) = g_{m_1} \cdot v_{gs_{1,2}}(t) + g_{m_2} \cdot v_{gs_{1,2}}(t)^2 + g_{m_3} \cdot v_{gs_{1,2}}(t)^3 + \ldots
\]

![Figure 1.6 Illustration of even-harmonic rejection in a balanced amplifier.](image)

If the two switching devices are provided with complementary inputs, they will generate currents in equal amplitude and opposite direction at the fundamental and odd-order harmonics, thereby circulating currents at those frequencies through the load. Assuming inputs \( v_{gs_1} = A \cos(\omega_{RF} t) \), \( v_{gs_2} = -A \cos(\omega_{RF} t) \), the currents flowing at the third harmonic would include contributions from the cubed terms, for example:
\[ g_m \cdot v_{ps1}(t)^3 = \frac{3}{4} A^3 g_m \left[ \cos(\omega_{RF} t) + \cos(3 \omega_{RF} t) \right] \]

\[ g_m \cdot v_{ps2}(t)^3 = -\frac{3}{4} A^3 g_m \left[ \cos(\omega_{RF} t) + \cos(3 \omega_{RF} t) \right] \]

However, at the even harmonics, the sources drive against one another, each seeing an open-circuit since no net current can be realized through the balanced load. It is this symmetry property that is widely exploited in differential signaling to reject common-mode noise, being applied here to provide the open-circuit conditions necessary for current-switching class-D amplification.

The behavior of an example tank circuit, which shorts odd-harmonic currents that are allowed to circulate in the CMCD transformer secondary without disturbing the termination at the fundamental, can be seen in Figure 1.7. The response of a parallel RLC circuit with 50 Ohm load (having \( Q=50\sqrt{C/L}=10 \)) is shown: the third, fifth, and higher harmonics see a near-short looking into this circuit, while the fundamental is matched to 50 Ohms. As previously mentioned, the structure of the CMCD allows absorption of device parasitics into the tank circuit. This is achieved by subtracting directly \( C_{ds} \), the drain-source capacitance across the output of each switching device, from the resonator capacitance \( C_0 \), since for each half-cycle capacitance \( C_{ds} \) of either transistor sits in parallel with the tank. Proper absorption of this capacitance ensures that the devices are switched on and off only when \( C_{ds} \) is discharged, a condition referred to in the literature as 'zero-voltage switching' (ZVS), seen in the waveforms in Figure 1.5.
1.1.2 The Symmetric CMCD

A challenge to the transformer-coupled CMCD topology is its use of a transformer balun before the parallel resonant circuit. This transformer is required to translate the current pulses flowing through the switches on the primary side without distortion to the secondary. However, designing such a transformer to work to even the third harmonic for an L-band design is nearly impossible [11]. Therefore, designs at high frequencies have migrated to the symmetric CMCD topology displayed in Figure 1.3 and detailed in Figure 1.8, in which the resonant circuit is placed between the switching devices before the balun. With this approach, the balun need only avoid distortion at the fundamental\(^4\) [6,12,13]. Before discussing the major factors impacting the efficiency of CMCD designs, a short analysis of the symmetric topology incorporating losses in the finite on-resistance of the switching transistor is repeated here to extend the introduction.

\(^4\) Additional topology innovations are discussed in Section 1.3.
of the prior section.

As seen in Figure 1.8, two RF chokes provide DC currents which are switched between the two transistors with 50% duty cycle as in the transformer-coupled case. When one switch is off, conducting no current, the total current $2I_{dc}$ must flow through the opposite switch. Therefore, the currents $i_1(t)$, $i_2(t)$ are again square, having peak $2I_{dc}$ and DC value $I_{dc}$. Let the current entering the tank and balun circuit be $i_3(t)$. Then $i_3(t)$ has zero average value and peak $I_{dc}$ with Fourier series representation:

$$i_3(t)=\frac{4}{\pi}I_{dc}\sum_{k=0}^{\infty} \sin\left((2k+1)\omega_{RF}t\right)$$

The resonator formed by $L_0$ and $C_0$ shorts the odd harmonic currents. Assuming the output balun to be 1:1 for this analysis, the load voltage then takes the form:

$$v_L(t)=\frac{4}{\pi}I_{dc}R_L\sin(\omega_{RF}t)$$
which again must be sustained between the drains of the switches. Taking $R_{ON}$ to be the resistance of the active devices in the triode/linear-resistance region, the drain-source voltages of the switches must be $2R_{ON}I_{dc}$ while they conduct. When they are cut off, they must sustain the reflected load voltage in addition to the $2R_{ON}I_{dc}$ drop across the opposing, conducting switch. Therefore, the drain-source voltages take the form:

$$v_{ds}(t) = \begin{cases} 2R_{ON}I_{dc} + \frac{4}{\pi}I_{dc}R_L\sin(\omega_{RF}t), & 0 \leq \omega_{RF}t < \pi \\ 2R_{ON}I_{dc}, & \pi \leq \omega_{RF}t < 2\pi \end{cases}$$

$$v_{ds}(t) = \begin{cases} 2R_{ON}I_{dc}, & 0 \leq \omega_{RF}t < \pi \\ 2R_{ON}I_{dc} - \frac{4}{\pi}I_{dc}R_L\sin(\omega_{RF}t), & \pi \leq \omega_{RF}t < 2\pi \end{cases}$$

which are again half-wave sinusoids comprised of DC, fundamental, and even harmonic components. The DC value of $v_{ds}(t)$ and $v_{ds}(t)$ must be $V_{DD}$. This knowledge may be used to find the DC current drawn by the circuit in terms of the supply voltage and circuit parameters by averaging either of the two $v_{ds}$ waveforms:

$$V_{DD} = \frac{1}{2\pi} \int_0^{2\pi} v_{ds}(\theta) d\theta = \frac{1}{2\pi} \left( 2R_{ON}I_{dc}\pi + 2R_{ON}I_{dc} \pi + \int_{\pi}^{2\pi} \frac{4}{\pi}I_{dc}R_L\sin(\theta) d\theta \right)$$

$$\Rightarrow I_{dc} = \frac{\pi^2}{4} \frac{1}{1 + \frac{\pi^2}{2} \frac{R_{ON}}{R_L}} \frac{V_{DD}}{}$$

This in turn can be used with knowledge of the load voltage to find an expression for the drain efficiency $\eta$ of the circuit as the ratio of output power $P_L$ to dissipated DC power $P_{DC}$:
\[ P_{DC} = 2I_{dc} V_{DD} = \frac{\pi^2}{2} \frac{1}{\frac{\pi^2}{2} \frac{R_{ON}}{R_L}} V_{DD}^2 \quad , \quad P_L = \frac{1}{2} \left( \frac{4}{\pi} I_{dc} \right)^2 R_L = \frac{8}{\pi^2} \left( \frac{P_{DC}}{2 V_{DD}} \right)^2 R_L \]

\[ \Rightarrow \eta = \frac{P_L}{P_{DC}} = \frac{2 P_{DC}}{\pi^2} R_L = \frac{1}{1 + \frac{\pi^2}{2} \frac{R_{ON}}{R_L}} \]

It can be seen that as the on-resistance of the devices go to zero, the drain efficiency approaches 100%, as expected. Additional factors degrade the efficiency of the CMCD in practice, many of which have been studied in detail elsewhere. These include:

- non-zero transition time of the active devices between their on and off states [14],
- switching losses due to parasitic inductance in series with the output terminals of the active devices [14],
- Ohmic losses in the resonator components and RF chokes [14,15].
- leakage of harmonic currents to the load [14],
- insertion loss of the output balun and any additional matching networks.
- switching waveform overlap due to bandlimiting from substrate parasitics and the high-frequency behavior of available surface-mount components [11,16,17].
- deviation from a half-cycle phase difference between drive signals [16].
- inaccurate modeling of non-linear device capacitance \( C_{ds} \) [18].
- drive power requirements (when considering power-added efficiency) [11,17,19].

Indeed, these issues make the CMCD a challenging and interesting amplifier to design.

---

5 Not only at the fundamental, but all higher harmonics, including any leakage at even harmonics.
6 Power-added efficiency (PAE) is defined as the ratio of output RF power minus input RF power to dissipated DC power. It therefore reflects more accurately an amplifier’s ‘true’ efficiency by incorporating drive power.
1.1.3 The Inverse Class-F Amplifier

The inverse class-F amplifier, an example of which is shown in Figure 1.9, is a single-ended SMPA class which employs the same terminating criteria as the CMCD. For this reason, the CMCD is often called 'push-pull inverse-F'. In the ideal inverse-F case displayed in Figure 1.9, the load network is made of infinitely many resonators which provide open-circuit terminations to the switch at the even harmonics, with odd harmonics being shunted to ground by the resonator at the load. Similar switching waveforms to the current-mode class-D result: square currents with half-sinusoidal voltage at the device. In practice, it is difficult to control the terminations beyond the third harmonic. Distributed approaches to realizing the tuning network have been studied intensely elsewhere [6,10,20] – an example of which can be seen in Figure 1.10. As is discussed in Section 1.2 of this thesis, the combination of two inverse-F PAs in the push-pull configuration has resulted in successful designs, beginning with Aflaki et al. in 2009 [13].

![Figure 1.9 Idealized inverse-F SMPA circuit](image)
1.2 Similar Designs in Open Literature

Many current-mode class-D designs have been published in the literature. These works are presented chronologically in Table 1.1. The first was shown by P.J. Baxandall, a famous name in audio electronics, who published results in 1959 coining the term 'class-D' to describe an oscillator he had designed [22]. Baxandall differentiated between two current switching and voltage switching topologies and noted the higher output power and efficiency capabilities of class-D circuits over class-C, the contemporary state-of-the-art (though Tyler had published the class-F topology at this time [23]). His bipolar designs operated around 100 kHz, providing efficiencies around 80%. By 1965 it was shown by Page, Hindson, and Chudobiak that pushing designs to tens of megahertz increased balun leakage inductance and capacitive device losses, though a 6.3W, 98% drain efficiency design at 1 MHz was published [24]. Chudobiak and Page later provided analysis concerned with devices in higher frequency class-D designs showing that maximum efficiency could be maintained until roughly a tenth of the switching device's transit frequency [25]. The class-BD amplifier, a hybrid of the B and D classes
demonstrated and analyzed by Martin in 1970 and experimented with at 1.9 MHz by Raab in 1974, was additionally shown by Raab in 1977 to theoretically provide 1.23 and 1.57 times the efficiency of traditional class-B at maximum and back-off power levels, respectively [26-29]. It was suggested here that the class-D topologies were good candidates for envelope elimination and restoration (EER) techniques, in which any amplitude modulation at the input to the power amplifier is removed by a limiter before amplification and superimposed on the high-power output by modulating the PA's power supply [30]. This technique and its contemporary derivatives have allowed switching PAs to meet the linearity requirements of today's communications standards, thus providing today's designer with a high-efficiency, linear option applicable beyond strictly phase modulating and frequency modulating systems.

The 'modern-era' of class-D RF PAs, so to speak, comes after many decades of progress in microwave transistor technology. Major gains, beyond the scope of this thesis, were made with the advent of laterally diffused MOSFETs (LDMOS), gallium arsenide (GaAs) MESFETs, pseudomorphic and metamorphic high-electron mobility transistors (pHEMTs, mHEMTs) and heterojunction bipolar transistors (HBTs). By the late 1990s and early 2000s it was clear that switching PAs could operate well into the GHz range. In 2001, the first conventional current-mode class-D PAs at UHF were published by Kobayashi et al., providing just under a Watt of power at 900 MHz with PAEs beyond 70% using packaged GaAs MESFETs [15]. The CMCD's previously mentioned ability to absorb device capacitances in order to achieve ZVS without limit was emphasized. This
option is limited with the class-E topology (which is designed for ZVS, zero-current-switching (ZCS), and zero-voltage-derivative-switching (ZVDS) conditions [7]) and entirely unavailable to voltage switching topologies. Additionally, GSM transmission (constant-envelope cellular communication) was demonstrated, and the viability of the CMCD in time-varying envelope systems was reiterated. Long, Yao, and Long then demonstrated in 2002 a high-power discrete LDMOS design providing 13 W at 1 GHz with 58% PAE, significant evidence of the benefit of the CMCD to wireless base stations using the dominant power transistor technology of the time [31]. These were followed by designs by Hung et al. (a low-power, integrated GaInP/GaAs HBT design at 700 MHz with innovative use of bondwire inductance in the harmonic termination network [14]) in 2004, a 50 W/56% PAE discrete LDMOS design at 1.8 GHz by Kim et al. in 2005 [12], and a 20 W/71% drain efficiency, LDMOS design at 1 GHz with exceptionally high gain for a SMPA (15.1 dB) by Nemati et al. in 2006 [32]. From 2007, research focused for the most part on moving designs to S-band and beyond, novel methods of improving harmonic terminations, demonstration of the CMCD on gallium nitride (GaN), and integration of envelope-modulated CMCDs in CMOS transmitters.

Gallium nitride CMCDs began at L-band with Aflaki et al. and Gustavsson et al. presenting designs with discrete GaN HEMTs and MESFETs, respectively [17,33]. Aflaki et al. showed 4 W/53% PAE at 1 GHz with 7.4 dB power gain. Gustavsson et al. were able to realize two amplifiers at 20 W/75% drain efficiency and 51 W/78% drain efficiency at 900 MHz for comparison with Nemati et al.'s LDMOS work from 2006.
saw the publication of the first two S-band CMCDs, both with GaN HEMTs, by Aflaki et al. and Al Tanany et al. [13,34]. Aflaki et al. demonstrated a 2.35 GHz, 8W, 65% PAE CMCD realized with a novel topology having identical termination conditions to the CMCD: the push-pull inverse class-F, which the authors called a 'distributed multiharmonic impedance transformation network'. In this sub-class, the two antiphase switching devices drive distributed terminations in the style of inverse class-F PAs and combine power at the balun before the load. Thus, this design can be seen as either a CMCD or two inverse class-F amplifiers, as previously discussed.

Distributed topologies hold many advantages: beyond L-band, it is difficult to find the low-loss, high-self-resonant-frequency surface-mount capacitors and inductors and low-loss, wideband surface-mount baluns necessary for a conventional CMCD design. Transmission line structures not only allow efficient designs at S-band and beyond, but they provide substitutes for lossy elements at L-band as previously demonstrated by Long et al. and Nemati et al., who substituted transmission line inductors into their designs. The 2008 work by Al Tanany et al. did the same, providing high power at S-band with 50 W/60.3% PAE at 2.14 GHz. This level of power and efficiency at S-band is surplus evidence of GaN's potential in the power electronics field. In the succeeding year, the push-pull inverse-F approach was applied to LDMOS by Schuberth et al. at 900 MHz, 25 W, 61.5% PAE and improved upon at lower S-band by Frebrowski and Boumaiza with 70.9% PAE, 18.6 W at 2.46 GHz on GaN [3,35]. In 2010, El Din et al. used GaN devices and a tunable harmonic termination network similar to push-pull
inverse-F to provide record 74% PAE at 7.4 W output power with the ability to improve
PAE by 25% over an 8 dB back-off range, while Stameroff, Pham and Leoni designed an
X-band push-pull inverse-F amplifier with 2 W output power, 63% PAE on GaAs
pHEMT at 10 GHz – the first of its kind in open literature [36,37]. Park et al. later used
bare die GaN HEMTs to achieve 3.5 W, 64.2% PAE at 3.3 GHz with the push-pull
inverse-F topology [38].

From 2010, the record shows some focus on CMOS integration with both
Chowdhury et al. and Nakatani et al. publishing numerous articles on designs with
CMCDs in polar transmitters [39-44]. In this branch of CMCD research, the benefits of
CMOS integration (cost reduction, adjacency to control and other sub-circuits) are seen
to outweigh the efficiency costs of using a technology with a lossier substrate. Chowdhury
et al. used several multiplexed, parallel CMCD switching stages to provide discrete
symbol amplitudes, achieving 151 mW peak power at 2.4 GHz, 44% drain efficiency
integrated with local oscillator distribution and filter circuits on a single die. Nakatani et
al. achieved a Watt-class CMOS PA as part of a transmitter with a buck-converter
envelope modulator (a voltage-mode class-D circuit, in fact) and digital linearity
compensation circuits with the use of stacked FETs to boost the breakdown voltage of
the CMCD switches. Today's CMOS processes, as opposed to LDMOS or GaN, have low
drain-source breakdown voltages which limit signal swing and therefore achievable
output power in PA designs. In CMOS current-mode class-D PAs which require
significant output power the designer is typically forced to step down the load impedance
with the use of transformers that tend to be increasingly lossy and narrowband as the transformation ratio increases. With the stacked FET technique, the 2011 design by Nakatani et al. achieved 46% PAE and 1 W output power at 750 MHz.

<table>
<thead>
<tr>
<th>Year</th>
<th>Author</th>
<th>Technology</th>
<th>Power Gain (dB)</th>
<th>Drain Efficiency (%)</th>
<th>PAE (%)</th>
<th>Output Power</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>1958</td>
<td>Baxandall</td>
<td>BJT, Discrete</td>
<td>79</td>
<td>95 mW</td>
<td>100 kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1965</td>
<td>Chudobiak</td>
<td>BJT, Discrete</td>
<td>98</td>
<td>6.3 W</td>
<td>1 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2001</td>
<td>Kobayashi</td>
<td>GaAs MESFET, Discrete</td>
<td>12</td>
<td>81.4</td>
<td>290 mW</td>
<td>900 MHz</td>
<td></td>
</tr>
<tr>
<td>2001</td>
<td>Kee*</td>
<td>NMOS, Discrete</td>
<td>17</td>
<td>85</td>
<td>1.1 kW</td>
<td>7 MHz</td>
<td></td>
</tr>
<tr>
<td>2002</td>
<td>Long</td>
<td>LDMOS, Discrete</td>
<td>14</td>
<td>60</td>
<td>13 W</td>
<td>1 GHz</td>
<td></td>
</tr>
<tr>
<td>2004</td>
<td>Hung</td>
<td>GaAs HBT, Integrated</td>
<td>12</td>
<td>78.5</td>
<td>.89 W</td>
<td>700 MHz</td>
<td></td>
</tr>
<tr>
<td>2005</td>
<td>Kim</td>
<td>LDMOS, Discrete</td>
<td>11.8</td>
<td>60</td>
<td>50 W</td>
<td>1.8 GHz</td>
<td></td>
</tr>
<tr>
<td>2006</td>
<td>Nemati</td>
<td>LDMOS, Discrete</td>
<td>15.1</td>
<td>71</td>
<td>20.3 W</td>
<td>1 GHz</td>
<td></td>
</tr>
<tr>
<td>2007</td>
<td>Aflaki</td>
<td>GaN HEMT, Discrete</td>
<td>7.4</td>
<td>65</td>
<td>4 W</td>
<td>1 GHz</td>
<td></td>
</tr>
<tr>
<td>2007</td>
<td>Gustavsson</td>
<td>GaN MESFET, Discrete</td>
<td>10.6</td>
<td>75</td>
<td>20.7 W</td>
<td>900 MHz</td>
<td></td>
</tr>
<tr>
<td>2008</td>
<td>Aflaki</td>
<td>GaN HEMT, Discrete</td>
<td>12.7</td>
<td>68</td>
<td>8.3 W</td>
<td>2.35 GHz</td>
<td></td>
</tr>
<tr>
<td>2008</td>
<td>Tanany</td>
<td>GaN pHEMT, Discrete</td>
<td>14.3</td>
<td>62.7</td>
<td>60.3</td>
<td>50 W</td>
<td>2.14 GHz</td>
</tr>
<tr>
<td>2009</td>
<td>Frebrowski</td>
<td>GaN HEMT, Discrete</td>
<td>12.7</td>
<td>75</td>
<td>18.6 W</td>
<td>2.46 GHz</td>
<td></td>
</tr>
<tr>
<td>2009</td>
<td>Schuberth</td>
<td>LDMOS, Discrete</td>
<td>15</td>
<td>63.5</td>
<td>25 W</td>
<td>900 MHz</td>
<td></td>
</tr>
<tr>
<td>2010</td>
<td>El Din</td>
<td>GaN, Discrete</td>
<td>21</td>
<td>74.6</td>
<td>74.7 W</td>
<td>1 GHz</td>
<td></td>
</tr>
<tr>
<td>2010</td>
<td>Chowdhury</td>
<td>CMOS, Integrated</td>
<td>44</td>
<td>151 mW</td>
<td>2.4 GHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2010</td>
<td>Stameroff</td>
<td>GaAs pHEMT, Discrete</td>
<td>10</td>
<td>70</td>
<td>2 W</td>
<td>10 GHz</td>
<td></td>
</tr>
<tr>
<td>2011</td>
<td>Park</td>
<td>GaN HEMT, Discrete Chip</td>
<td>10</td>
<td>77.2</td>
<td>3.5 W</td>
<td>3.3 GHz</td>
<td></td>
</tr>
<tr>
<td>2011</td>
<td>Nakatani</td>
<td>CMOS, Integrated</td>
<td>51</td>
<td>46</td>
<td>1 W</td>
<td>750 MHz</td>
<td></td>
</tr>
</tbody>
</table>

*this design is not a CMCD, but is closely related.

Table 1.1 Current-mode class-D designs presented in open literature.

1.3 Design and Thesis Overview

This thesis documents the design and demonstration of a push-pull inverse-F form of the current-mode class-D power amplifier specified for 1 GHz operating frequency and 1 W output power. A single die with CMCD switching stage and driver stage was
fabricated using a gallium arsenide pHEMT process with half-micron gate lengths. The die was bonded to an open quad-flat no-leads (QFN) package [45] and mounted on microwave substrate with microstrip harmonic terminations, surface-mount input/output baluns and SMA connectors, decoupling and bias networks. Specifically, the following objectives for the design were proposed:

1. Design a CMCD on 0.5 μm gate length GaAs pHEMT technology with at least 1 W of simulated output power and drain efficiency greater than 65% at 1 GHz with all circuit losses modeled. The switching devices should not exceed 2 millimeters of gate periphery to ensure the accuracy of non-linear models provided by the foundry.

2. Design a driver stage to be integrated with the CMCD which will provide the two-stage amplifier with a power gain greater than 20 dB while keeping the simulated power-added efficiency of the two-stage design above 60%.

3. Design a printed circuit assembly (PCA) for amplifier testing which includes baluns, bias terminal blocks and decoupling, microstrip harmonic terminations, and input/output SMA connectors. The PCB, chip, and QFN will be fabricated and assembled by commercial manufacturers with any adjustments made by the author at the University.

4. Characterize the fabricated amplifier by measuring the output power, power gain, frequency response and amplifier efficiency for comparison with simulated expectations.

The design, whose block diagram is shown in Figure 1.11, was prepared with Agilent's Advanced Design System (ADS) simulation and layout software. ADS was used to perform harmonic balance simulations with both Angelov and Parker-Skellern large-
signal models of the GaAs pHEMTs provided by the foundry [46-49]. Additional on-chip passive models include metal-insulator-metal (MIM) capacitors, spiral inductors, back-vias\(^7\), on-die transmission lines, bond pads and inter-layer metal transitions. The scattering parameters of all off-chip surface-mount components, provided by their respective manufacturers, were included in simulation, as well as accurate models of PCB microstrip.

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**Figure 1.11** Block diagram of the power amplifier documented in this thesis.

Terminal blocks supply DC power to the board such that the two amplifier stages may share bias supplies or decouple for troubleshooting and optimization. The input and...
output baluns are M/A-COM MABA-007871-CT1A40 transmission line baluns, chosen for their low insertion loss (0.3 dB), low phase unbalance (0.1 ± 4°) and wide bandwidth (5 to 3000 MHz) [50-52]. Knowledge of the output balun response to the third harmonic of the design frequency (to 3 GHz here) is essential when designing the distributed termination network: as discussed in detail in the prior sections, the drain efficiency of the class-D design depends upon approximating short-circuit terminations at the odd-order harmonics and open circuits at the even harmonics. A low-pass filter (matching network) comprised of surface-mount components sits before the input balun to eliminate any harmonic content fed to the circuit from the desktop signal generator. To summarize, the balun converts the single-ended input signal to two antiphase signals feeding the driver stage on-chip by microstrip, which feeds the switches terminated by the output network, balun and load.

The succeeding chapters of this thesis focus on the integrated circuit design, board design, lab testing, and potential application of the IC in a power mixer circuit. Chapter 5, which documents work on the mixer circuit, is written in a self-contained fashion, with discussion of the motivation and background for that work included there. Chapter 2 details the methodology and simulation results of the integrated circuit design. Chapter 3 focuses on the PCB design, a critical part of the overall PA, while Chapter 4 documents expected performance and realities measured in a University laboratory.
CHAPTER 2
INTEGRATED CIRCUIT DESIGN

This chapter presents the detailed design of the GaAs integrated circuit (IC) in four sections. Section 2.1 provides an overview of the large-signal device models used for simulation. Section 2.2 details the CMCD stage design of the IC. Section 2.3 shows the first-pass design of the driver stage, and Section 2.4 shows the final design iterations of the amplifier MMIC.

2.1 A Note on Simulation Models

Before the IC design is detailed, this section provides a brief overview of the large-signal models used for circuit simulation throughout the design. Many switching power amplifiers have been designed with rudimentary transistor models in which the active device is treated as a switch with an 'on' and 'off' resistance and relevant parasitics (typically only the output capacitance $C_{ds}$) as is shown in Figure 2.1. Modeling the transistor in this manner for harmonic balance simulation often leads to convergence problems since the equations describing the switch conductance have discontinuous derivatives. For the design described in this thesis, two more sophisticated large-signal models from the foundry were available.

The first model, fitted to process measurements (on devices only 20% the size of the devices in this design), is based on the Parker-Skellern model – a MESFET model
eventually extended to cover the transconductance nonlinearity seen with HEMTs [47,48]. The second is a more recently measured Angelov-based model (also developed for MESFETs and extended to cover phenomena particular to HEMTs) based on measurements of devices 30% the size of the switching pHEMTs in this thesis design [46,49]. The Parker-Skellern model was the primary simulation model throughout the design phase of this project, with the Angelov model becoming available toward the end of that work – it was therefore used as a check on prior results and a 'second opinion' when comparing simulation to measurement. These two models describe the transistor behavior with equations having continuous derivatives and, of particular importance to this design, attempt to capture the curvature of the drain-source conductance in the knee region with high accuracy. Important features of the models are discussed briefly in the following sections.

![Figure 2.1 Simple switch model of a transistor [16].](image)

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8 In either case, the device layout for model extraction is unknown to the author.
2.1.1 Parker-Skellern Model

The topology of a generic Parker-Skellern model is seen in Figure 2.2. The gate-drain and gate-source diodes represent the Schottky gate, with diode capacitances $C_{gd}$ and $C_{gs}$.$^9$ Large-signal behavior is described with continuous derivatives, and thereby improved simulation convergence and prediction of intermodulation distortion, by modifying the controlled-resistance equations describing a JFET to cover all regions of operation by continuous transformations of its inputs (the terminal voltages). The modification begins with the equation for intrinsic drain current in terms of gate and drain terminal voltages $v_{GT}$, $v_{DT}$:

$$i_d = \beta v_{GT}^q [1 - (1 - \frac{v_{DT}}{v_{GT}})^q]$$  

(Eq. 2.1.1.1)

where controlled-resistance operation below the knee voltage is modeled with a fitting

---

$^9$ Parameters for fitting bias-dependent behavior of these capacitances are included in the model. The S-parameters of the model have been shown to match measurement well [47].
parameter $Q$ (typically 2) for $0 < v_{DT} < v_{GT}$, while cut-off and saturated operation are traditionally modeled by discontinuous transitions which set $i_d = 0$ for any $v_{GT} < 0$ and $i_d = \beta v_{GT}^Q$ for any $v_{DT} \geq v_{GT}$. The Parker-Skellern model removes these hard transitions.

This is done by mapping the terminal voltages into Equation 2.1.1.1 using smooth functions with $0 < v_{DT} < v_{GT}$ always true; each transform maps a range of effective values into Equation 2.1.1.1 without causing any high-order discontinuities. For instance, $v_{DT}$ is restricted to $[0, V_{sat}]$ by the transformation of an effective value $v_{DP} \in [0, \infty)$ using:

$$v_{DT} = \frac{1}{2} \sqrt{(v_{DP} \sqrt{1+Z}+V_{sat})^2 + Z V_{sat}^2} - \frac{1}{2} \sqrt{(v_{DP} \sqrt{1+Z}-V_{sat})^2 + Z V_{sat}^2}$$  \hspace{1cm} (Eq. 2.1.1.2)

When $v_{DP}$ is large, $v_{DT} \approx V_{sat}$. When $v_{DP}$ is small, $v_{DT} \approx v_{DP}$ and the second and third derivatives of this transform with respect to $v_{DP}$ are zero – the transform therefore has no effect on Equation 2.1.1.1 in the controlled-resistance region. Parameter $Z$ controls the shape of the transition to controlled-current where $v_{DT} \approx V_{sat}^{10}$. This approach to modeling the controlled-resistance and knee region is an improvement over those models which use a hyperbolic tangent function to describe the conductance there (as is done in the Angelov model): Figure 2.3 shows a comparison of this model with measurement and the hyperbolic tangent method, presented by Parker and Skellern in their original publication, of drain current, its first derivative, and second derivative.

$V_{sat}$ itself is selected by a smooth function to be the lesser of $v_{GT}$ and the velocity saturation potential.
Figure 2.3 Drain current and its derivatives for the Parker-Skellern model (−), hyperbolic tangent (− -), and MESFET measurement (•, ×) [47].

Additional transformations allows for independent control over the shape of the power-law description of drain current in controlled-resistance and controlled-current regions. For sub-threshold conduction, the model never allows the intrinsic current source to completely turn off but rather maps values of gate-source voltage below cut-off into $v_{GT} \in (0, \infty)$ as the logarithm of a quantity slightly larger than unity – giving exponential decay of drain current close to cut-off. Breakdown, occurring at large negative gate-source and gate-drain potentials, is modeled entirely by the diodes extrinsic to this non-zero current source (seen in Figure 2.2), and the smooth transform function used for mapping the gate-source potential, like Equation 2.1.1.2, does not effect the model of conduction above cut-off. It improves modeling of drain current and its derivatives near cut-off over 'conditional cut-off' models in which this behavior is omitted.
or discontinuous.

In addition to providing continuous descriptions of large-signal behavior, the Parker-Skellern model includes several time-averaged features which allow the model to 'respond' to changing bias, power dissipation, and rate-dependent phenomena. Of particular importance to this design is the model of power dissipation in the channel: a time-average power dissipation is calculated from the instantaneous drain current and drain-source voltages. The time scale over which the power is averaged is parameterized. Given some calculated average power $P$, the conductance is reduced with $i_{ds}=i_d/(1+\delta P)$ where $\delta$ is a model parameter related to the temperature coefficient of current reduction and the thermal resistance of the channel. Similar averaging techniques are used to calculate the time-average terminal voltages and adjust the bias point appropriately, as well as account for the natural dispersion of transconductance at high frequencies. The response of the model to these time-averaged quantities is similarly parameterized for fitting to measured quantities.

2.1.2 Angelov Model

![Figure 2.4 Generic Angelov model schematic](53)
The topology of a generic Angelov model is seen in Figure 2.4, excluding the parasitics at the device terminals. As previously mentioned, the intrinsic current source models the drain current using hyperbolic tangent functions [46]. These functions model the behavior throughout a large-signal swing with good accuracy\(^\text{11}\) and the 'bell-shape' of HEMT transconductance is captured. Simulator convergence is improved since all derivatives are continuous, as in the Parker-Skellern model. Likewise, diode equations describe the Schottky gate structure and its reverse breakdown. Unlike the Parker-Skellern model, capacitances \(C_{gs}\) and \(C_{gd}\) are modeled with their own hyperbolic tangent functions to describe their bias dependence. These capacitances, as well the device parasitics, are fitted to measurement for good S-parameter agreement\(^\text{12}\). The drain current is modeled as the product of two functions dependent on \(V_{gs}\) and \(V_{ds}\), respectively:

\[
I_{ds} = I_{ds} (V_{gs}, V_{ds}) = I_{pk} (1 + \tanh(\Psi))(1 + \lambda V_{ds}) \tanh(\alpha V_{ds})
\]

\[
\Psi = P_1 (V_{gs} - V_{pk}) + P_2 (V_{gs} - V_{pk})^2 + P_3 (V_{gs} - V_{pk})^3 + \ldots
\]

where \(I_{pk}\) is the drain current at maximum transconductance and \(V_{pk}\) is the corresponding gate-source voltage\(^\text{13}\). \(\lambda\) and \(\alpha\) capture channel length modulation and set the saturation voltage point, respectively. \(\Psi\) is a power series fit to measurement with coefficients \(P_n\) which dictate the dependence on \(V_{gs}\). Typically, only \(P_1\) is necessary for fairly good accuracy – that is, \(\Psi\) is usually close to a linear function of

---

\(^{11}\) Though the Angelov model does not purport to capture sub-threshold and cut-off behavior precisely.

\(^{12}\) Bias point \(V_{gs} = 0\), \(V_{ds} = 0\) is used to measure the parameters fitting \(C_{gs}\) and \(C_{gd}\), for instance.

\(^{13}\) \(V_{pk}\) shows some dependence on \(V_{ds}\) in the saturated regime and considerable dependence in the controlled-resistance regime. These relationships are modeled with additional equations discussed in [46].
\(V_{gs}\), with \(P_3\) often included [46]. Of importance to an SMPA design, the remaining terms play a role in determining the curvature of the drain conductance in the controlled-resistance region. Example model and measured results from the original publication by Angelov et al. can be seen in Figure 2.5.

The Angelov model was extended by its authors to include heating effects, soft breakdown, and conductance dispersion [49]. The model used in this thesis design, however, takes into account only the soft breakdown effects. Soft breakdown is considered as the sharp increase in drain current observed in HEMTs well below drain-gate breakdown. This behavior has been found to have dependence on the gate-source voltage despite any breakdown currents flowing in the gate. The approach taken by Angelov et al. to extend the model is to incorporate an additional term \(L_{sb}\) in the drain-source current expression such that:

\[
I_{ds} = I_{pk} (1 + \tanh (\Psi)) \tanh (\alpha V_{ds}) (1 + \lambda V_{ds} + L_{sb})
\]

\[
L_{sb} = L_{sb0} \left[ \exp (L_{sd1} V_{dgs} + \ldots) - 1 \right], V_{dgs} = \frac{V_{ds} - K_{ng} V_{gs}}{V_{tr}}, L_{sd1} = L_{d1} (1 - L_{gs} V_{gs})
\]

\(L_{sb0}\) and \(L_{sd1}\) match the model to experiment, with the option of including additional terms to increase accuracy. \(V_{dgs}\) is a normalized term that captures the effect of both gate-source and drain-source voltages on soft breakdown currents.
Figure 2.5 Angelov model predictions (–) at $V_{ds} = 1\ V$, 2 V shown with measurement (●) at $V_{ds} = 1\ V$ on a 200 micron by 0.15 micron device. Drain current, $\Psi$ function, transconductance, and its derivative are shown [46].

2.2 Switching Stage Design

The design begins with the switching stage, which was first drafted as an idealized symmetric CMCD to identify upper bounds on achievable output power and efficiency as well as design criteria for the driver stage. The following sub-sections describe this work, which was finalized after the layout and stability studies discussed in Section 2.4.

2.2.1 Switch Sizing and Vdd Selection

The first design task was the choice of switching transistor size and the power supply voltage of the output stage to meet the specifications outlined in Section 1.3. As discussed, the on-resistance – and therefore the size – of the switching devices is a major
contributor to the power lost in the circuit and should be minimized. Analysis of the CMCD waveforms\(^\text{14}\) shows that the output power, drain efficiency \(\eta\), and peak drain-source voltage across each switch in the symmetric CMCD topology can be bounded by:

\[
P_o \leq \frac{\pi^2 V_{dd}^2}{2 R_L} \eta \quad \eta \leq \frac{1}{1 + \frac{\pi^2 R_{ON}}{2 R_L}} \quad V_{ds,\text{pk}} \leq \pi V_{dd}
\]

accounting only for static losses in \(R_{ON}\), where \(R_{ON}\) is the device on-resistance, \(R_L\) is the load resistance, and \(V_{dd}\) is the power supply voltage. Since \(V_{dd}\) has no bearing on the efficiency, it can be chosen with the output power specification and the roughly 16 V breakdown voltage of the pHEMT process as consideration: if no impedance transformation is made to the 50 Ohm load, 1 W of output power requires \(V_{dd}\) greater than 3.3 V but not more than 5 V to prevent damage to the devices by the expressions for output power and peak drain-source voltage above. Therefore, 4.7 V was chosen to leave margin. The reader should note the trade-off between output power and drain efficiency given a target load resistance when designing a CMCD: as \(R_{ON}/R_L\) goes to zero (if the load resistance were transformed upward from the perspective of the switches), the output power \textit{decreases} for a fixed \(V_{dd}\) and \(R_{ON}\) while the efficiency \textit{increases}. Since high efficiency was desired with 1 W of output power, no transformation was made to the target 50 Ohm load. In addition, the commercially available transmission line balun with best insertion loss and bandwidth up to the third-harmonic was 1:1 in 50 Ohms.

\(^{14}\) In addition to that of Section 1.2.2., presented well by Grebennikov, Sokal, and Franco [6].
Since the design is intended to have a highly efficient, high-gain first stage, the PAE and drain efficiency will be nearly equal, since:

$$PAE = \frac{P_{OUT}}{P_{IN} + P_{DC}} = \eta \left( 1 - \frac{1}{G_p} \right)$$

where $G_p$ is the scalar power gain. The devices may therefore be sized to maximize the drain efficiency of the output stage while ignoring their drive power requirements (this burden now being placed on the DC consumption of the driver stage). On the advice of modeling engineers at the foundry, two millimeters of gate periphery was set as an upper bound for model accuracy. Therefore, the switching stage is comprised of devices formed by ten 200 by 0.5 micron gate fingers, whose total on-resistance is 1.05 Ohms. This places the drain efficiency maximum at 90.6%, and the maximum achievable output power at 1.975 W. It will shortly be seen that other circuit losses degrade these numbers significantly.

### 2.2.2 Output Capacitance Extraction

In order to work with a first-pass CMCD design that has properly aligned waveforms, an approximation of the output capacitance $C_{ds}$ of the pHEMT model for absorption into the tank circuit was deduced from transient simulations. Simulated current pulses fed into the drain terminal with the device in cut-off were used to compute the stored charge $Q_d$ at the drain in order to take rough\(^{15}\) estimate $C_{ds} \approx \frac{\Delta Q_d}{\Delta V_{ds}}$, as in Figure 2.6. The resulting transient waveforms are shown in Figure 2.7, with the

---

15 Extremely rough, the network between the drain and source is certainly not a simple capacitor.
estimated capacitance plotted in Figure 2.8. By specifying an initial condition on the drain voltage of 0 V, the estimate is taken as:

\[
C_{ds} \approx \frac{\int_0^{2 \text{ ns}} I_{ds}(t) \, dt}{\max |V_{ds}(t)|}
\]

It can be seen that as the device moves from cut-off to conduction beyond \( V_{GS} = -1.4 \, V \), the channel behavior changes and currents begin to leak from the output capacitance.

**Figure 2.6** Simulation schematic for estimation of device output capacitance.
Figure 2.7 Transient simulation results for several gate-bias pinch-off levels: current forcing in blue, voltage response in red (Parker-Skellern model).

Figure 2.8 Computed approximate output capacitance $C_{ds}$ of 2-mm pHEMT model seen in Figure 2.6, estimated from response shown in Figure 2.7.

This approximate capacitance, taken in future simulations as 0.8 pF, was checked by simulating a symmetric CMCD with a lumped element resonator slightly detuned. That circuit, which employs ideal voltage source drivers, is shown in Figure 2.9. The resulting optimum drain efficiency, around 0.8 pF of absorbed device capacitance, is shown in Figure 2.10. It should be noted that for a 1 GHz design and 50 Ohm load, a tank circuit
of Q greater than ten, which provides a very good odd-harmonic short, requires approximately 32 pF of resonator capacitance and 0.77 nH inductance. The estimated

\( C_{ds} \) shifts the resonance of the tank only 1.2% from 1 GHz if left unabsorbed yet the simulated efficiency decrease of 3% is not insignificant.

![Figure 2.9](image1.png) 1 GHz symmetric CMCD with loss-less resonator and zero driver source impedance for \( C_{ds} \) estimate check. Parameter 'Cout', subtracted from the resonator capacitance, was varied.

![Figure 2.10](image2.png) \( C_{ds} \) estimate check: drain efficiency of circuit of Figure 2.9 computed from harmonic balance results with absorbed output capacitance 'Cout' varied.
2.2.3 Simulated Source Pull

With $C_{ds}$ estimated to ensure a properly tuned tank circuit, the optimum output impedance and available power of the driver stage at the fundamental frequency could be estimated by simulated source pull of both switches simultaneously. A schematic example is shown in Figure 2.12: the simulation was repeated at several available power levels shared by the two source tuners driving the switches in antiphase with identical source impedances. Likewise, the gate-source bias condition of the two switches is identical. The resulting PAE maxima using the Parker-Skellern large-signal model, all of which are displayed with output power\(^{16}\) contours in Appendix B of this thesis, are tabulated in Table 2.1 with an example seen in Figure 2.11. It can be seen in Figure 2.12 that these simulations take into account resonator components of finite Q: the data used for those losses (inductor Q, capacitor ESR) was taken from the datasheets of commercially available components [54,55]. In addition, the three-port scattering parameters (a .s3p file) of the transmission line balun are seen between the resonator and 50 Ohm load: typical losses associated with the output balun are therefore taken into account. However, at this point in the design, the DC feed inductors at the gate and drain terminals of the switching stage are left ideal and the IC packaging, on-chip transmission lines and passives, and PCB traces are not modeled. In this way, the source-pull simulations give a preliminary look at the achievable PAE of a fairly idealized switching stage design in the presence of some of the RF losses typical of later design stages.

\(^{16}\) It is seen in Appendix B and Figure 2.11 that the output power specification, requiring greater than 30 dBm simulated power, is easily met. In addition, the PAE and output power contours are concentric.
The data show power-added efficiencies in the range of 74.7 to 76% to be likely upper bounds on the results of later design iterations. Since a gate-source bias closer to zero may lead to dangerous forward-biased gate-drain and gate-source junctions, a gate-source bias around -0.7 to -0.6 V and 12 dBm available drive power were taken as suitable targets for the next phases of the design.

**Figure 2.11** Source-pull simulation result at 12 dBm available power per driving transistor, -0.7 gate-source bias voltage.

<table>
<thead>
<tr>
<th>Gate-Source Bias (V)</th>
<th>-0.7</th>
<th>-0.6</th>
<th>-0.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>74.7</td>
<td>75.6</td>
<td>76</td>
</tr>
<tr>
<td>10</td>
<td>75.1</td>
<td>75.8</td>
<td>75.9</td>
</tr>
<tr>
<td>11</td>
<td>75.4</td>
<td>75.8</td>
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<td>12</td>
<td>75.5</td>
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<td>75.4</td>
</tr>
<tr>
<td>13</td>
<td>75.2</td>
<td>75.1</td>
<td>75</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Power Available (dBm)*</th>
<th>-0.7</th>
<th>-0.6</th>
<th>-0.5</th>
</tr>
</thead>
</table>

*Power available per tuner – two are used.

**Table 2.1** Tabulated PAE maxima (%) from source-pull results seen in Appendix B.
Figure 2.12 Source-pull simulation schematic showing shared gate-source bias and driving source tuners.
Generally, the results show the optimum PAE point lying at a source reflection coefficient of roughly $0.814 \pm 114^\circ$ (impedance $7.257 + j31.99$) across bias and power levels. After designing the driver stage to this specification, it was best to check that $0.814 \pm 114^\circ$ is a source-stable reflection coefficient from the perspective of the switches\textsuperscript{17}. However, linear stability tests do not completely describe the stability of switching power amplifiers. The stability criteria of the switching stage were estimated by observing source stability circles of a single switch at several bias points: in the 'idle' state ($V_{ds}=4.7$ V, $V_{gs}=-0.6$ V here) – where the RF drive signal is off, or small with the output stage operating linearly in push-pull service – as well as the DC states which roughly comprise the transient states between the 'on' and 'off' switching states\textsuperscript{18}. These states were taken as $V_{ds}=1$ V with $V_{gs}$ taken from the set \{-1.4, -1, -0.6, -0.2, 0.2, 0.6, 1\} V. Since there is no power gain with the device cut off, the behavior in the 'off' half-cycle of switching (in which there is a large voltage swing with little current) is left out of this stability analysis. Stability circles were studied at high frequencies (1 GHz to 10 GHz in steps of 1 GHz) and low frequencies (100 MHz to 1 GHz in steps of 100 MHz) providing a rough view of the stability criteria of the 2-mm devices throughout their non-linear swing at several frequencies of interest – all results being gathered in Appendix C of this thesis. Considering only the fundamental frequency, those source stability circles show clearly that the optimum termination for PAE is not linearly stable at the 'idle'

\textsuperscript{17} It was also altered for load stability with respect to the driver-stage pHEMTs, described in Section 2.4. The design iterations are easier presented chronologically.

\textsuperscript{18} Small-signal stability at each state of a large-signal, non-linear swing may not imply non-linear stability. This approach is an estimate beyond the linear stability study at the 'idle' bias point, with any instabilities being prospectively fixed in the lab during prototype testing.
bias point $V_{DS} = 4.7$ V, $V_{GS} = -0.6$ V and for several of the transient states. Figure 2.13 reiterates the result at the 'idle' bias point, with the optimum PAE point marked and circled in the unstable region.

![Source Stability Circles](image)

**Figure 2.13** Source stability circles of 2-mm device at the linear bias point with optimum PAE termination at the fundamental highlighted.

With these results as consideration, the target driving impedance was moved to $16.5 + j18.25$ Ohms ($\Gamma = 0.553 \pm 136^\circ$), its reflection coefficient being highlighted with orange in the stable region of Figure 2.14 – shown again with the circles at the 'idle', linear-operation bias point. This selection is stable for all bias points seen in Appendix C. The reader will note that a study of the load stability circles of the driver devices has not yet been presented. In addition, the network which delivers this source impedance to the switch gates is not yet synthesized – therefore, its high and low-frequency behavior has not yet been quantified. Those issues are treated in detail in the subsequent sections.

With the target driving impedance at the fundamental identified, the simulation was repeated with a fixed source termination in order to observe the time-domain waveforms with the stabilization: that result, giving $\text{PAE} = 74.4\%$ (a cost of under 2%
PAE to stabilize) at gate-source bias -0.6 V and available drive power $P_{av} = 12$ dBm, shows clearly the current-mode class-D response, as seen in Figure 2.15\(^{19}\).

Figure 2.14 Source stability circles of 2-mm device at design frequency and higher harmonics at the 'idle' bias point with source-stable termination highlighted.

Figure 2.15 Switching waveforms resulting from narrowband stable source impedance $Z_S = 16.5 + j18.25$, $V_{GS} = -0.6$ V, $P_{av} = 12$ dBm.

2.3 Driver Stage Design

Having identified the preliminary source termination for the switching stage, a

\(^{19}\) With the Angelov model, which tended to show more loss, simulation showed 66.9% PAE under these conditions. In addition, source pull simulations with the Angelov model (results of which are not shown in this thesis) give nearly identical criteria for optimum PAE compared to the Parker-Skellern model.
first-pass driver stage design which minimizes its own dissipated power was studied. The final driver stage design, whose half-circuit is shown in Figure 2.16 with its drain-source waveforms\(^{20}\), was found to best be implemented with a saturated class-C stage: a switchmode driver would require a complex harmonic tuning network which would incur excessive loss when realized on-chip, while the synthesis of optimum driving impedances from the perspective of the switching stage may not coincide with the synthesis of optimum harmonic terminations and bias feeding for a switching driver. A class-A driver would not be optimally efficient, while saturated class-C provides more output power than a single-ended class-B for the same bias current and conduction angle (i.e. more efficiency). The subsequent section discusses the first-pass design beginning with the criteria established in Section 2.2.

Figure 2.16 (a) Simplified driver schematic with off-chip decoupling shown; (b) response at device output in full-PA simulation.

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\(^{20}\) These show saturation: the current spikes down when the device moves past the knee region to small drain-source voltages. There is negative swing in which current is conducted from the grounded source with a small contribution (300 μA) from the slightly forward-biased gate-drain junction of the device.
2.3.1 First Pass

A class-A driver with minimal on-chip losses and minimal complexity, to be used in class-C service in succeeding design phases, was drafted given the target available power and source impedance established in Section 2.2. The topology is seen in Figure 2.17. The driving pHEMT is treated as a linear current source with quantities of interest labeled: $R_{ds}$ represents the drain-source resistance of the pHEMT, $R_{L_1}(\omega)$ represents the DC and frequency-dependent losses of spiral inductor $L_1$, and $ESR_{C_1}(\omega)$ represents the frequency-dependent losses of MIM capacitor $C_1$. Both $L_1$ and $C_1$ have frequency-dependent reactive parts, captured in models provided by the foundry\textsuperscript{21}. The off-chip pi-section shown previously in Figure 2.16 prevents high-frequency current flow from the desktop DC supply, while the additional on-chip 10 pF serves to prevent a high inductance path between the off-chip decoupling and the spiral.

![Figure 2.17 Schematic representation of driver circuit.](image)

\textsuperscript{21} The model and data used to refine the design of this inter-stage matching network is proprietary.
As can be inferred from Figure 2.17, inductor $L_1$ does not function strictly as a DC choke: it feeds DC drain bias to the driving device while tuning the real and imaginary parts of impedance $Z_s(\omega)$ in concert with capacitor $C_1$. As is the case in most semiconductor processes, spiral inductor losses far outweigh MIM capacitor losses (that is: $R_{L_1}(\omega) >> ESR_{C_1}(\omega)$) at 1 GHz, thereby simplifying the degrees of freedom chosen iteratively to deliver a source termination tuned closely to a given target. The source impedance is easily calculated as:

$$Z_s(\omega) = \left[ R_{L_1}(\omega) + j\omega L_1(\omega) \right] || R_{ds} + ESR_{C_1}(\omega) + \frac{1}{j\omega C_1(\omega)}$$

Output resistance $R_{ds}$ is high enough to be ignored for the smaller driving pHEMTs. Therefore, to design the 16.5 + j18.25 Ohms termination found to be source-stable for the switching stage, for example, it suffices to choose a spiral inductor $L_1$ which has roughly 16.5 Ohms loss at 1 GHz whose reactance remains greater than the target j18.25 Ohms at 1 GHz – the remaining deficit between the synthesized termination and the target is tuned by the negative reactance of capacitor $C_1$, which contributes only a small loss at 1 GHz. In other words, for a target source impedance $A + jB$ at $\omega_0$:

$$A \approx R_{L_1}(\omega_0) + ESR_{C_1}(\omega_0), \quad B \approx \omega_0 L_1(\omega_0) - \frac{1}{\omega_0 C_1(\omega_0)}$$

This approach was used to consecutively design the optimum-PAE termination\(^\text{22}\), size the driving devices assuming both stages to operate on a 4.7 V DC supply, perform layout

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\(^{22}\) Note that this was done before tuning the termination to be source-stable for the class-D stage.
and stability studies, and finally simulate a source-pull of the refined two-stage design to match to the input balun. These results were used to retrofit simulations (detailed in the next section) with transmission lines on-die, back-vias to die ground, package parasitics, bondwires, and off-chip components.

As discussed, the driving devices were initially sized by treating them as linear sources operating on a 4.7 V bias supply. The available power $P_{\text{av}}$ of each driver at some frequency $\omega_0$ can be written as, c.f. Figure 2.17:

$$P_{\text{av}}(\omega_0) = \frac{i_o^2 R_L(\omega_0)^2 + \omega_0^2 L_1(\omega_0)^2}{8 \Re \{Y_s\} + \frac{\omega_0^2}{8 R_L(\omega_0)^2} + ESR_C(\omega_0)}$$

in Watts, where $i_o$ represents the peak AC current swing of the active device in Amperes at frequency $\omega_0$. The minimally sized device, and therefore most efficient for class-A use, which can deliver this current $i_o$ at the fundamental is that which is biased to a DC drain-source current equal to $i_o$ on the 4.7 V supply and is able to deliver $2i_o$ peak-to-peak current. The devices can then be roughly sized for a given termination $Z_s$ with knowledge of the desired available power.

The efficiency of the drivers is increased by operating them as saturated class-C amplifiers; a class-C stage driving current pulses with peak $2i_o$ at 50% conduction angle will provide the same power as this intermediate class-A design, with overdrive providing an additional, marginal increase in power when saturated. In either case, the output impedance of the driver at higher harmonics will play a role in the efficiency of

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23 For conduction angles other than 50%, this similarity with class-A is not the case.
the switching stage. As discussed, complexity in the interstage matching network on-chip was not desired for this design – therefore, the output impedance of the class-C driver stage was stabilized but not optimized at the harmonics. The effect of driver saturation, for the portion of the cycle in which the driving device swings past the knee region into triode, was not studied for its effect on efficiency or stability: for this portion of the cycle, the switching device is cut off, with no means of providing gain. By this reasoning, stability is not likely to be affected, while simulations in addition did not show a significant effect on the efficiency of the switching stage.

The first-pass driver design began with the optimum-PAE source termination before any stabilization and the specified available drive power of 12 dBm. The target source reflection coefficient from Section 2.2 was $0.814 \pm 114^\circ$, corresponding to $7.257 + j31.99$ Ohms. It is desired to synthesize a termination close to this optimum. One solution is a spiral of nominal inductance 8.8 nH and 5.42 pF MIM capacitor, giving a simulated terminating impedance roughly $3.385 + j26.6$ Ohms. That structure is shown in the context of the two-stage first-pass simulation prepared for another source-pull trial, with driving devices sized to 75 micron periphery to supply $i_o$ of 12 mA (12 dBm $P_{av}$), in Figure 2.18. The Smith chart of Figure 2.19 shows the optimum PAE reflection coefficient at the fundamental with that used in this iteration of the design superimposed upon the prior results of the simulated source-pull – it is nearly optimal. The response of the design at this stage is illustrated by varying the drive power with the source tuners set to 50 Ohm driving impedance – those simulation results, showing a 1 to 2% cost in
efficiency with the addition of the driver stage, are shown in Figure 2.20. In this case, the class-C and class-D stages both operate on drain supply voltage 4.7 V with gate-source bias -0.6 V.

Figure 2.18 First-pass inter-stage match shown with 75 micron driving devices, 2-mm output stage, resonator, output balun and source tuners for two-stage source pull simulation.
2.4 Layout Study and Design Iterations

The preliminary IC layout, drawn in Agilent ADS, can be seen in Figure 2.21. All bond pads, transmission lines, back-vias, and metal layer transitions were added to
future schematic simulations, models being taken from a kit provided by the fabricator\textsuperscript{24}. In addition, a first selection and layout of surface-mount decoupling, bias feeding, and output resonator components external to the IC was done. This allowed for the dimensioning of bondwires between the die and QFN package, since the design could be placed within the context of the external circuitry to establish a pin-out. In this manner, both the IC layout and initial PCB layout were treated together, as can be seen in Figure 2.22, where the bondwire locations are shown in orange, the QFN land pattern is shown in wireframe green, and mock-up PCB traces connecting to the package from external circuitry are shown with teal. The scattering parameters of the surface-mount components external to the chip were included in subsequent simulations.

\textsuperscript{24} Features by the spiral inductors were spaced three substrate heights (300 microns) from the metal comprising the inductors to ensure the accuracy of the simulation model – predictable behavior of these inductors is critical to the performance of the PA.
Figure 2.21 Preliminary integrated circuit layout approximately 2.4 by 1.5 mm: differential input shown at bottom, bias connections at sides, with switching stage at top.

Figure 2.22 Preliminary layout with mock-up PCB metal and bondwire locations shown.
2.4.1 Refined Simulation

A screenshot of the refined simulation schematic with sections of interest labeled is shown in Figure 2.23 below. Each sub-circuit is subsequently detailed.

Figure 2.23 Refined simulation schematic.
Figure 2.24 shows a single switching pHEMT and surrounding circuitry from the refined schematic – this excerpt is the half-circuit of the switching stage. Vias to ground are shown connected between the device source and the on-chip ground node 'Int_GND'. Models of each bond pad leading to the output network, each being 70 μm square, are seen at right. The gate-source DC bias is fed in with an 0402-sized inductor from Coilcraft, seen at the bottom of the figure. That connection transitions through the package and bondwire models section, leading to the bond pad shown connecting to the
pHEMT gate by transmission line and three, parallel layer transitions (from top metal to gate metal). These features can be seen in the preliminary artwork, an excerpt highlighting them is shown in Figure 2.25 below.

Figure 2.25 Artwork excerpt showing gate-bias transition to die (bottom), top-metal transmission lines (red/blue) and transitions to gate-metal layer (yellow). Bondwires are represented with orange, with one leg of the differential output seen at right after the pHEMT switch.

25 On-die transmission lines were modeled as 5.5 micron-thick gold (σ=4.1·10⁷ S/m) on 4-mil thickness GaAs (εᵣ=12.9).
Figure 2.26 shows the bondwire and package model section of the schematic. At left, the differential input signal arrives on nodes 'In_P' / 'In_N' and transitions to the die with each leg using a bondwire pair. The bond pads by the switch drains, half of which were shown in Figure 2.24, transition the signal off-chip at right, with each pad taking one leg of a bondwire pair. In total, the eight on-chip pads connect to four leads on the package frame (the differential output is seen as nodes 'Vext_P' and 'Vext_N'): this approach was taken to minimize the inductance and losses between the switches and resonator. Lastly, the top and bottom of the figure show one bondwire pair for each driver supply, and one bondwire for each gate bias line to the switches.

![Schematic representation of bondwire and package simulation models](image-url)
The wire bonds use the Philips-TU Delft model as gold (\( \sigma = 4.1 \cdot 10^7 \text{S/m} \)) of 1 mil diameter [56]. All bondwire pairs are modeled with 25 micron separation. The input signal bonds are 1.5 mm length, while the remaining bonds are 20 mil (0.508 mm) length. As will be discussed in Chapter 3, the bondwire model captures roughly the geometry of the real bonds, which are shown with the final artwork at the end of this chapter.

The output network is shown in Figure 2.27. All components are represented by their scattering parameters. The DC feed inductors, chosen for their low DC loss (6.2 mOhms), are shown at the top of the figure, with a single 100pF decoupling capacitor before the DC supply.

The resonator is comprised of five surface-mount capacitors and a single surface-mount inductor. These components were chosen due to constraints on the self-resonant
frequency and losses of available commercial products. Spreading the resonator currents over several components lowers those losses\textsuperscript{26}. Two 100 pF capacitors are used to AC-couple the resonator to the transmission-line balun from M/A-COM before the load.

The driver stage half-circuit is shown with the switch of Figure 2.24 in Figure 2.28. The dimensions of the transmission lines connecting the driving device to the inter-stage matching components can be seen in Figure 2.29. The transition off-chip to the drain supply can be seen to the left of the spiral inductor in the two figures: the decoupling network external to the chip is seen at node 'Driver1_Vaa_Ext', comprised of several 100 pF capacitors with a 100 nH inductor isolating high-frequency currents from the DC supply. The artwork corresponding to the sub-circuit in these figures is displayed in Figure 2.30 for comparison. That figure shows the transmission line feeding the gate of the driving device, which is part of the input network shown in Figures 2.31 and 2.32. The artwork corresponding to the input section is shown in Figure 2.33.

\textsuperscript{26} As discussed in Chapter 3, preliminary board layouts showed the electrical length between these many components to be an additional design consideration – eventually, the symmetric CMCD approach was discarded for the push-pull inverse-F topology.
Figure 2.28 Schematic representation of driver half-circuit with switching stage half-circuit.
Figure 2.29 Finer view of driver half-circuit.
Figure 2.30 Die artwork showing driver device (bottom right) and spiral inductor with bondwire transition to package.
Figure 2.31 Refined input network: input signal is fed to T-section filter and split by input transmission line balun (left). Transmission lines between transition to die and driver gates are modeled.
Figure 2.32 Refined input network shown with focus on transmission line half-circuit between input bond and driver gate.
Figure 2.33 Artwork excerpt showing differential input lines to driver gates.

The simulation results of interest for this intermediate, refined schematic are illustrated by Figures 2.34 through 2.36. It can be seen that the addition of microstrip lines, input filter, decoupling and 'real' resonator components has cost: peak PAE is 68.2%, the linear gain has dropped several dB, and the switching waveforms show less ideal harmonic content (some of which is likely due to the inaccurate extrapolation of their scattering parameters to the higher harmonics by the simulator). It can be seen in Figure 2.36 that the driver is able to sustain the desired current swing with some saturation. The driver sizing is therefore settled, with any changes left to tuning of its drain supply voltage and gate bias in a lab setting.
Figure 2.34 Gain, output power, and efficiency vs. input power for refined simulation.

Figure 2.35 Switching waveforms of refined simulation at high-efficiency point.
2.4.2 Stabilization and Final IC Design

With the preliminary artwork and schematic updates detailed in the prior section, the reflection coefficient looking into either side of the interstage matching network could be studied for stability. As discussed in Section 2.2, the source termination of the switching stage was adjusted first in light of the stability circles shown in Appendix C (peak PAE now simulating 64.9%). That alteration, requiring the inter-stage components to be changed to nominal values 1.8 pF and 14.7 nH from 5.42 pF and 8.8 nH, is illustrated in Figures 2.37 and 2.38. Figure 2.37 shows the two terminations from 100 MHz to 10 GHz in 100 MHz steps with stability circles at the bias point, black dots being the original termination and blue dots being the refined termination. It is evident from the low-frequency stability circles of Figure 2.37(b) that the altered termination is...
still unstable at 200 MHz – this is true of the final choice of termination network as well, but was not discovered until after the design was measured: oscillations occurred in the lab and were fixed by altering the gate bias networks of the switching stage – this is detailed in Chapter 4. Figure 2.38 illustrates the method of simulating these reflection coefficients. The package and bond models are included in the simulation but not shown in the figure. The driver is taken as an open circuit: it is relatively small, with the design frequency being low enough for its $C_{ds}, C_{dg}$ to be ignored.
Figure 2.37 Behavior of switching stage source termination in 100 MHz steps before (black) and after (blue) alteration. High frequencies (a) and low frequencies (b) with relevant stability circles at $V_{ds} = 4.7$ V, $V_{gs} = -0.6$ V. The unstable region is inside the circles.
Figure 2.38 Annotated schematic showing elements comprising the source termination of the switches.
The inter-stage matching network was further studied for load stability from the perspective of the driver stage devices. Similar to the prior work, the load stability circles of the driving devices were studied at the bias point and throughout the transient states that comprise their saturated class-C swing (those circles are displayed in Appendix D). The load reflection coefficient was simulated with two approaches: once in the context of the entire IC design, as seen in Figure 2.39, and again with the switching stage device replaced with an RC model. This RC model, seen in Figure 2.40, was derived from prior simulations with the switching device compressed (at the high-efficiency operating point of the PA). In this way, the load stability of the driver stage was studied in the linear operating region as well as the high-efficiency region in which the switching devices are saturated.

The reflection coefficient in the two cases is shown in Figure 2.41 with the stability circles at the bias point: black dots denote the reflection coefficient with the RC gate model, while blue dots show the linear-region model. It is desired to stabilize the driving device in both cases. However, as can be seen in the example, this termination shows considerable mid-frequency instability between approximately 260 MHz and 1 GHz.
Figure 2.39 Annotated schematic showing elements comprising the load termination of one driver.
Figure 2.40 Annotated schematic showing elements comprising the load termination of one driver with the 2-mm switch modeled as a 4.129 Ohm resistor and 5.14 pF low-pass network between its gate and source terminals.
Driver load reflection coefficient extracted using approaches seen in Figure 2.39 and Figure 2.40. Device biased to 4.7 V, -0.6 V, with the unstable region being inside the circles.

In order to partially stabilize the load termination for the driving device (that is, to stabilize it at least at 1 GHz with both models of its load), the inter-stage matching components were again tuned. Figure 2.42 shows the resulting reflection coefficients – it can be seen that the termination at 1 GHz has been moved a small amount to the stable, lower half-circle of the Smith chart with the low-frequency instability problems remaining. Therefore, possible in-band oscillations and probable low-frequency oscillations were expected with the lab prototype using this last alteration to the inter-stage matching network: a 1.5 pF MIM capacitor and 17.5 nH spiral inductor\textsuperscript{27}. The resulting reflection coefficient from the perspective of the switching devices is seen in

\textsuperscript{27} At this time the low-frequency instability of the switches was unknown. These driver stability problems were left to be shown in the lab, since de-Q'ing different sub-circuits in advance would necessarily limit the efficiency of the design.
Figure 2.43 in blue with that of the prior step in black – it has only slightly changed, with simulations of the full PA showing 63.1% peak PAE with a necessary decrease in linear gain, as seen in Figure 2.44.

![Load Stability Circles of 75-um pHEMT Shown with Load Terminations](image)

**Figure 2.42** Driver load reflection coefficient extracted using approaches seen in Figure 2.39 and Figure 2.40 after final alteration. Device biased to 4.7 V, -0.6 V, with the unstable region being inside the circles.
Figure 2.43 Source reflection coefficient of class-D switching devices before (black) and after (blue) load-stabilization of driver device at 1 GHz at (a) high and (b) low frequencies.
A final step in the integrated circuit design, before the finalization of the layout, is the tuning of the input matching network\textsuperscript{28} for driver stability and increased linear gain. The input network before this last change is shown in Figure 2.45: the signal flows through a low-pass filter\textsuperscript{29} (a matching network) with 3 dB cut-off frequency approximately 1.5 GHz (composed of the 8.2 nH inductor, 10 pF and 3 pF capacitor) and is split by the input balun. 100 pF capacitors AC-couple each leg of the split signal, while 100 nH inductors are used to feed the gate bias to the first amplifier stage. These high-pass networks, on each leg of the differential inputs to the chip, were altered to adjust the source reflection coefficient seen by the driving devices.

\textsuperscript{28} This network is off-chip. However, its tuning is carried here because of its relation to the source-stability of the drivers.

\textsuperscript{29} This input filter, before the balun, was designed incorrectly and later fixed. Figure 2.45 shows the original version, which was not properly matched at 1 GHz at its two ports.
To identify a target source reflection coefficient for the driver stage, a simulated source-pull was again undertaken. The reader will remember that the simulation has already taken into account the transmission lines, packaging, and bonding structures between the source tuners and the drivers, as seen in Figure 2.46, which shows the source tuners driving the entire PA. A sample of the source-pull results with the switching stage at the onset of saturation (at total available input power 6 dBm, c.f. Figure 2.44) is shown in Figure 2.47, showing a roughly 3% possible increase in PAE due to increased driver stage gain and thereby marginally increased output power at this single simulation point: the 0.5 dBm range in output power which covers the Smith chart in the figure indicates that a better gain match at the driver source shifts the compression point of
the PA to a lower input power – essentially shifting the output power curve of Figure 2.44 to the left. In other words, with a better match at the driver, the PA simulates well into compression at 6 dBm input power.

Figure 2.46 Schematic showing simulated source pull of entire PA from package terminals.
Figure 2.47 Simulated two-stage source-pull results with PA in high-efficiency, saturated regime. Maximum output power/PAE termination marked with black.

A source reflection coefficient close to the optimum was achieved by transforming the impedance presented by the balanced ports of the input balun\(^30\), resulting in the reflection coefficient shown in Figure 2.48. The termination is presented with the source stability circles of the driver at the bias point (the driver source-stability circles along the large-signal class-C swing are collected in Appendix E). The AC-coupling were replaced with 2.2 pF capacitors from ATC, while the choke inductor is replaced with a 9 nH inductor from Coilcraft – the burden of shorting high-frequency currents now being placed on the decoupling network at the DC supply side of those inductors. With this alteration and an updated input filter\(^31\), the peak simulated PAE is 64.9% with linear gain increasing to 39.7 dB, as shown in the performance curve of Figure 2.49.

\(^{30}\) The balun is a 1:1 transmission line transformer balun designed to 50 Ohms – the balanced ports are assumed here to each present 25 Ohms to a virtual ground.

\(^{31}\) The corrected filter shows -26.6 dB return loss and 0.133 dB insertion loss at 1 GHz with 3 dB cut-off frequency 2.3 GHz. A 3.3 nH inductor, 2 pF shunt capacitor, and 2.2 nH inductor lead to the balun.
This concludes the simulation portion of integrated circuit design, with the final selection of off-chip components and the development of push-pull inverse class-F harmonic terminations detailed in Chapter 3. The finalized integrated circuit layout, which shows the additional 10 pF added to the drain supply node of the driver stage as well as clean up of the circuit symmetry is shown in Figure 2.50, with one of the die used for lab testing displayed in Figure 2.51.

![Redesigned Driver Source Reflection Coefficient Shown with Source Stability Circles](image)

**Figure 2.48** Retuned source reflection coefficient seen by driver devices, shown with stability circles of the 75-μm device at the bias point (4.7 V, -0.6 V). The stable region is outside of the circles.

![Gain (dB), Output Power (dBm), and Efficiency of Refined 2-Stage Design with Stability, IMN, and Input Filter Modifications](image)

**Figure 2.49** Performance curve with driver source-reflection coefficient and input filter updated.
Figure 2.50 Final integrated circuit layout of the two-stage amplifier prepared with Agilent ADS. The die is 2.56 mm by 1.8 mm before dicing.
Figure 2.51 Micrograph showing fabricated die mounted in open-QFN package with bonds, solder connections to PCB seen at edges.
CHAPTER 3
PRINTED CIRCUIT BOARD DESIGN

This chapter documents the design of the printed circuit board (PCB) on which the packaged integrated circuit, described in detail in the prior chapter, was mounted for lab evaluation. Section 3.1 provides a detailed overview of the PCB layout and its important features. Section 3.2 documents the design method for the microstrip harmonic termination network at the amplifier output, and Section 3.3 details the power supply decoupling networks.

3.1 Overview

The layout of the PCB can be seen with annotations in Figure 3.1 – it is roughly 3.8 by 2.4 inches, fabricated on two-layer Rogers material of 31 mil thickness with 1 oz. copper layers (1.4 mil thickness). Land pads for the components are demarcated by the green solder-mask layer in the figure: end-launch SMA jacks for the input and output signals can be seen at the top and bottom, the QFN-packaged chip is seen centered.

The stub terminations at the amplifier output were kept 30 mils from the nearby gate bias feed networks to limit crosstalk between the two amplifier stages. In addition, the ground lines from the terminal blocks are alternated in a signal-ground-ground-signal fashion, as can be seen in Figure 3.1, such that ground runs adjacent to the stubs, terminating any electric fields which would extend from the PA output back to the bias
feeds. The many vias from top metal to the solid ground plane on the bottom of the board ensure paths of minimal inductance for current flow to and from the decoupling networks, as well as a clean path to ground underneath the QFN.

The decoupling passives, all capacitors of which are from American Technical Ceramics' 600S series, and all inductors of which are from Coilcraft's 0603HP and Air Core series, were chosen for their low ESR (equivalent series resistance), high Q, high SRF (self-resonant frequency), and availability of S-parameters for simulation [55,57,58]. Since 0603-sized components were preferred for easy hand soldering, the SRF of available capacitors was relatively limited – the large arrays of capacitors decoupling the switch drain supplies are necessary to provide sufficient capacitance with good SRF. The two wire-to-board terminal blocks which distribute DC power from the left and right of the packaged chip are the Phoenix PSTM 0.5/8-HH-2,5-SMD-R44 [59]. Land pads for the surface-mount components are prepared with adjacent gaps in the top copper layer to generate hot points at which there is little copper to spread heat, thereby steering the flow of solder for easier manipulation in the lab. A photograph of the final, assembled design is seen in Figure 3.2.
Figure 3.1 PCB design, prepared in Agilent ADS, with yellow annotations. Silkscreen is shown in white, top copper in red, and solder-mask layer in green. Board dimensions are shown with white annotations along the board edge.
Figure 3.2 Assembled board with input, output and bias connected. Some of the rework discussed in Chapter 4 can be seen.
3.2 Output Network

As discussed in the first chapter of this thesis, the design of the output network loading the CMCD is critical to achieving high efficiency: the network should provide the desired load at the fundamental and approximate short-circuit terminations at the odd harmonic frequencies, the even-harmonic open-circuit terminations being satisfied by the balanced nature of the circuit. Preliminary layout studies of the termination design described in Chapter 2, in which a resonant tank circuit was used, showed sensitivity to distributed circuit effects from the intervening transmission lines between components: reducing the losses in the tank circuit required several parallel, low-ESR capacitors, all of which would require some minimum distance from one another to allow for hand soldering. To simplify the design, a structure derivative of prior work with push-pull inverse class-F style terminations was developed [3,13,35,37,38].

In most class-F and inverse class-F PAs using distributed terminations, a combination of open and short-circuit stub networks of varying complexity and interconnection are used to tune the third harmonic and beyond. In this design, distributed terminations control the fundamental and third harmonic frequencies, while the fifth and higher harmonics are left uncontrolled. This approach trades simplicity and board space for the efficiency gains provided by terminating the additional harmonics (however, a perfect fifth-harmonic termination improves the theoretical maximum efficiency only 2-4%) [8].
3.2.1 Push-Pull Inverse Class-F Harmonic Terminations

A preliminary to designing harmonic terminations is understanding the interface between the two switching transistors and the load. That network was modeled with knowledge of the transistor output capacitance, bond pads, bondwires, package parasitics, and output balun, as seen in Figure 3.3, shown with an additional tuning capacitor loading the pins of the QFN package before the output balun.

![Simulation Diagram](image)

**Figure 3.3** Simulation for estimation of optimal tuning reactances at fundamental, 3rd harmonic.

The reader will recognize the 0.8 pF device capacitance previously absorbed into the resonator of the traditional CMCD design. The wire bonds are again simulated with the Philips-TU Delft model available in ADS as gold (\( \sigma = 4.1 \cdot 10^7 S \)) of 1 mil diameter, 20
mil length, in pairs of two with 25 μm separation to reflect accurately the geometry of the assembled package [56]. The shape of the individual bonds is modeled as three commensurate sections: one launching off the die at a height of 100 μm (the die is 100 μm, or 4 mils, thick) reaching a height of 200 μm, one horizontal section at that height, and one final section reaching down to the lead frame at a height taken as 0 μm, where the package lead frame transitions down to potential PCB traces seen as nodes 'Vext_N' and 'Vext_P' in Figure 3.3 – this is a rough approximation of the curvature of the real bonds, later to be refined by three-dimensional, finite-element method (FEM) simulation models. The three-port scattering parameter representation of the commercial transmission-line transformer balun before the single-ended load is included for accurate accounting of its effects on the terminations.

To estimate the tuning network reactance necessary to provide optimal terminating conditions to the active devices, the tuning capacitor C5 of Figure 3.3 was varied, while the reflection coefficient and input impedance seen from the balanced port between the drains of the two devices was simulated over frequency. ADS allows non-physical (i.e. negative) capacitance values to be used in this parameter sweep, thereby allowing positive and negative reactance to be added between 'Vext_P' and 'Vext_N'. The parameter sweep results can be seen in Figures 3.4 and 3.5: the magnitude of the third harmonic termination, the input impedance from the switches' perspective at 3 GHz, appears to be minimized at 6.2 pF and the fundamental is matched best to 50 Ohms at -0.4 pF (the target load identified in Chapter 2 to achieve good efficiency and 1
W output power). These correspond to an optimal termination network which provides 
-j8.557 and j397.887 Ohms-reactive at those frequencies, respectively.

![Graph](image1.png)

**Figure 3.4** Full-sweep (a) and magnified (b) simulation results at the third harmonic (3 GHz) for tuning capacitance parameter sweep.
These tuning reactances were first synthesized with single open-circuit stubs\(^\text{32}\) loading each leg, as seen in Figure 3.6. The return loss at the fundamental and the magnitude of the third harmonic termination from the perspective of the switches is seen against stub length for several stub widths in Figures 3.7 and 3.8. The width shared by the two stubs controls their quality factors, and with increasingly wider lines the match at the fundamental is increasingly detuned. It can be inferred from these results that very thin stubs under an inch in length are appropriate for the terminating criteria at both the fundamental and third harmonic – however, in a real implementation of the circuit these stubs would be terminated with an RF choke which feeds DC currents to the switching stage; thinner stubs would incur unnecessary ohmic loss at DC and decrease the efficiency of the PA. Therefore, it was desired to realize a network which limits this DC loss by using fairly wide stubs \textit{without} detuning the power match at the

\[\text{Figure 3.5 Full-sweep simulation results at the fundamental frequency (1 GHz) for tuning capacitance parameter sweep.}\]

\[\text{The microstrip substrate was 2-layer Rogers RT/duriod 5880 31-mil thickness, 1 oz. copper, modeled properly for these lines with } \epsilon_r=2.2, \mu_r=1, \tan\delta=0.0009 \text{ at 10 GHz.}\]
fundamental. Studying a set of smaller feed inductances (stub terminations) and optimizing the stub length for 50 mil-width lines was the chosen course.

**Figure 3.6** Tuning network substituted into the simulation of Figure 3.3 for study of single, open-circuit harmonic tuning stubs on each leg of the push-pull output.

**Figure 3.7** Magnitude of 3rd harmonic termination impedance vs. open-circuit stub length for several stub widths.
Figure 3.8 Magnitude of fundamental return loss vs. open-circuit stub length for several stub widths.

The modified simulation schematic for testing several ideal stub-terminating inductors can be seen in Figure 3.9, with simulation results showing third harmonic termination and fundamental return loss versus stub length for several inductance values in Figures 3.10 and 3.11. Several inductor choices can simultaneously match the fundamental and 3rd harmonic termination criteria well over a set of stub lengths. After a search for high-Q, low-DC-resistance (DCR) surface-mount inductors with suitable self-resonant frequency, the 4 mOhm DCR, 1.65 nH, 0906-2_LB Air Core inductor from Coilcraft was chosen [55]. The high Q of the feed inductors is critical, as significant RF current will flow through them. Using the scattering parameters provided by Coilcraft for this component the simulation was finally repeated to choose the optimal stub length of 1220 mils, giving an estimated 3rd harmonic termination of magnitude 1.642 Ohms and return loss at 1 GHz of -22.913 dB, as seen in Figures 3.12 and 3.13.

Since the scattering parameters of ten sample baluns were available for simulation, an estimate of process variation effects due to the output balun could be
simulated prior to fabrication of the PCB. That simulation showed an average third harmonic termination of magnitude 1.732 Ohms, no more than 1.975 Ohms, and an average return loss at the fundamental of -22.092 dB and no worse than -18.827 dB. Simulation of the full PA design, as was described in Chapter 2, using this terminating structure shows a class-D stage with average 74.8% drain efficiency (minimum 73.8%) across these baluns using the Parker-Skellern pHEMT model, with the full PA achieving 70-71.6% PAE$^{33}$. These are therefore generous upper bounds on the efficiency of the lab prototypes in this work. Finally, the simulated gain performance with these prototyped terminations can be seen in Figure 3.14 – in this case, the balun scattering parameters were fixed to those which were used throughout Chapter 2, with the results showing 39.5 dB linear gain, 30.9 dBm saturated output power, and peak PAE 71%.

Figure 3.9 Tuning network substituted into the simulation of Figure 3.3 for study of single, inductively-loaded stubs on each leg of the push-pull output.

$^{33}$ With the addition of the refined decoupling networks described later in this chapter.
Figure 3.10 Magnitude of 3rd harmonic termination vs. stub length for several feed inductances.

Figure 3.11 Fundamental return loss vs. stub length for several feed inductances.

Figure 3.12 Magnitude of 3rd harmonic termination vs. stub length for available low-DCR inductor.
3.2.2 Finite Element Method Study

A three-dimensional FEM model was solved for the S-parameters of the harmonic terminations for comparison with the results described in the prior section. The 3D model, shown from several perspectives in Figures 3.15 through 3.20, includes accurate
geometry and physical constants for the following: top die metallization at the switch drain nodes, gold bondwire pairs in standard JEDEC shape, 4 millimeter open-air QFN package with plastic molding\textsuperscript{34}, aluminum lead frame, paddle, and GaAs die as well as the board and its copper transmission lines and vias. Board vias and metal traces adjacent to the microstrip terminations, detailed in Figure 3.15 and Figure 3.20, were added to a second, refined model to estimate possible coupling effects between those features and the output terminals of the switching devices.

The 6-port S-matrix results (two ports at the stub DC feeds, two ports at the switch drains, and two ports at the AC-coupling/balun solder pads) were used to extract the impedance seen differentially from the CMCD output by simulating this 6-port with feed inductors in place, thereby allowing the computation of the mixed-mode scattering parameters of a 4-port [60,61]. With the 0.8 pF output capacitance of the devices included, the differential-mode parameters were computed, thereby giving a 2-port network to be simulated in series with the balun and load in order to derive the impedance seen by the balanced CMCD. These results are displayed in Figures 3.21 and 3.22: the return loss and magnitude of the input impedance looking into the terminations are shown against frequency for both the schematic-level model of the prior section and the differential response extracted from the FEM model with and without board features adjacent to the stub terminations. Another look at balun variation was also possible: across the ten balun files, the FEM model which ignores the additional board features shows maximum return loss at the fundamental of -16.6 dB averaging -18.9 dB, with a

\textsuperscript{34} A modified 3D model, the original provided freely by Amkor at http://www.amkor.com.
third harmonic termination under 1.92 Ohms averaging 1.805 Ohms. With the adjacent board features accounted for, the maximum return loss was -16.59 dB averaging -18.86 dB with third harmonic termination under 8.64 Ohms averaging 8.55 Ohms. It is clear from Figure 3.22 that the third harmonic termination is detuned by the presence of the adjacent metal and vias, the minimum termination impedance now occurring 100 MHz below the intended 3 GHz minimum. This result warrants redesign of the stub lengths, but this refined FEM model was studied after the board was fabricated.

The simulated switching waveforms using FEM data to model the output terminations are shown in Figure 3.23, where the effect of designing a network limited to the third harmonic can be seen when compared to tank circuit terminations, as was shown previously in Figure 2.15 for example. The performance curves of the PA simulated with the refined FEM model taking the place of the microstrip model of the prior section are seen in Figure 3.24, where the maximum simulated PAE has dropped to 68.3%, saturated output power to 30.28 dBm, and linear gain is now 39.59 dB. Table 3.1 below compares these metrics in the schematic-level and two FEM-level cases. Table 3.2 describes the stack-up of the FEM model in detail.

<table>
<thead>
<tr>
<th>Model</th>
<th>Max. PAE (%)</th>
<th>Max. Output Power (dBm)</th>
<th>Linear Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Schematic (Microstrip)</td>
<td>71</td>
<td>30.9</td>
<td>39.5</td>
</tr>
<tr>
<td>FEM</td>
<td>72.2</td>
<td>30.32</td>
<td>39.63</td>
</tr>
<tr>
<td>Refined FEM (Adjacent Features)</td>
<td>68.3</td>
<td>30.28</td>
<td>39.59</td>
</tr>
</tbody>
</table>

Table 3.1 Comparison of PA performance between schematic-level and FEM-level termination models.

35 In all cases the output balun file is the same as used throughout the IC design. The slight increase in PAE between microstrip and first FEM model is likely due to the FEM models showing better 5th harmonic terminations.

36 The bondwires were 0.5 mm length with 1 mil diameter, \( \sigma=4.1\times10^7 \text{ S/m (gold)} \), with their interiors included in the 3D mesh.
Figure 3.15 3D model used for FEM solution of harmonic termination design, full view. Board shown in teal, its microstrip in green, vias with yellow. Package model (seen at center), shown detailed in the succeeding figures.

Figure 3.16 3D model used for FEM solution of harmonic termination design, magnified view of QFN package. Package molding shown as semi-transparent black, lead frame as solid red and blue, GaAs die as transparent pink, bondwires in orange, and microstrip breakout in green on teal RT/Duroid material.
Figure 3.17 3D model used for FEM solution of harmonic termination design, magnified wireframe view of QFN package shown to illustrate grounded paddle connection (green PCB metal layer) with PCB through-vias (yellow).

Figure 3.18 3D model used for FEM solution of harmonic termination design, magnified view of QFN package shown to illustrate package stackup: aluminum lead frame modeled as two layers (red, blue) with molding layer, open air cavity with die (wireframe pink).
Figure 3.19 3D model used for FEM solution of harmonic termination design, side view illustrating PCB/QFN stack-up and bondwire geometry.

Figure 3.20 3D model used for FEM solution of harmonic termination design, magnified view showing one microstrip stub feed and adjacent board metal included for estimation of coupling effects.
Figure 3.21 Predicted harmonic termination network return loss vs. frequency using microstrip model and 3D FEM results with and without adjacent board features.

Figure 3.22 (a) View of impedance magnitude and (b) reflection coefficient of termination using microstrip model and 3D FEM results with and without adjacent board features from 500 MHz to 5 GHz.
Figure 3.23 Simulated switching waveforms across several output baluns using the Parker-Skellern device model and refined FEM model.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Thickness</th>
<th>Physical Constants</th>
</tr>
</thead>
<tbody>
<tr>
<td>Free space</td>
<td>Infinite</td>
<td>$\varepsilon_r = 1, \mu_r = 1$</td>
</tr>
<tr>
<td>Die Metal</td>
<td>1 $\mu$m</td>
<td>$\sigma = +\infty$ Siemens/m</td>
</tr>
<tr>
<td>Die Substrate</td>
<td>4 mils</td>
<td>$\varepsilon_r = 12.9, \tan \delta = 0.0028$ (GaAs)</td>
</tr>
<tr>
<td>Lead Frame Molding*</td>
<td>100 $\mu$m</td>
<td>$\varepsilon_r = 3.7, \mu_r = 1, \tan \delta = 0.009$ (Plastic)</td>
</tr>
<tr>
<td>Lead Frame Metal*</td>
<td>100 $\mu$m</td>
<td>$\sigma = 3.77 \times 10^7$ Siemens/m (Aluminum)</td>
</tr>
<tr>
<td>PCB Metal</td>
<td>1.4 mils</td>
<td>$\sigma = 5.97 \times 10^7$ Siemens/m (Copper)</td>
</tr>
<tr>
<td>PCB Substrate**</td>
<td>31 mils</td>
<td>$\varepsilon_r = 2.2, \mu_r = 1, \tan \delta = 0.0009$ (RT/Duroid 5880)</td>
</tr>
<tr>
<td>Ground Plane</td>
<td>Infinite</td>
<td>$\sigma = +\infty$</td>
</tr>
</tbody>
</table>

*these layers are co-located vertically  **PCB vias modeled as perfect electrical conductor

Table 3.2 3D FEM model layer stack-up.

Figure 3.24 Simulated PA performance with refined FEM model of output terminations.
3.3 Decoupling Networks

It is important to briefly document the layout and response of the power supply decoupling networks at this stage of the design, as will be evident from the content of Chapter 4: altering them was of crucial importance to stabilizing the PA in the lab. Indeed, the self-resonance of both the inductors and capacitors selected became a problem. This section reviews those four DC feed networks.

3.3.1 Vdd Decoupling Networks

The simulation schematic for characterizing the impedance of the drain supply decoupling network used for each of the class-D switches is shown in Figure 3.25, the layout is shown in the excerpt of Figure 3.26. This network must provide a low impedance to ground with little loss in order to preserve the harmonic terminations of the PA. A total of fifteen 0603-sized components are used to accommodate 870 pF of nominal capacitance. Eight 100 pF capacitors are used to decouple the lower end of the spectrum (i.e. the fundamental) – these have a specified SRF of under 2 GHz with 60 mOhm ESR at 1 GHz. Seven 10 pF capacitors, which have an SRF specified at 4 GHz and have again 1 GHz ESR of 60 mOhms are used to shunt currents up to the third harmonic. Using numerous capacitors divides high frequency currents in order to lower RF losses and provides room for rework if necessary (swapping or adding other elements for low-frequency or high-frequency decoupling, or de-Q'ing). In addition, the layout of these components adds another roughly 3 pF of capacitance between the top and bottom
(ground) metal of the PCB, which is modeled in Figure 3.25. The simulated impedance of this decoupling network is seen in Figure 3.27, where the effect of low-SRF components is seen by the peaking under 2 GHz. The simulated voltage ripple of the two supplies when the PA is in saturation (where current swing through the switches is highest) can be seen in Figure 3.28, where the simulator assumes a perfect DC feed at the terminal-block side of the power supply connection.

![Figure 3.25 Schematic model showing power decoupling network of switch drain supply isolated for simulation.](image1)

![Figure 3.26 PCB artwork excerpt with decoupling network circled.](image2)

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37 It should be noted both that the third harmonic termination seen by the devices increases 0.64 Ohms to a simulated 9.19 Ohms with these more realistic decoupling networks in place at the feeds (the previous sections of this chapter assumed perfect decoupling in presenting the termination design) and that this simulation does not model distributed effects between the capacitors.
Figure 3.27 Response of switch Vdd decoupling network vs. frequency.

Figure 3.28 Time-domain display of simulated voltage ripple of switch Vdd supplies.

The network between the terminal blocks and drain-supply QFN leads of the driver stage are shown schematically in Figure 3.29 with a layout excerpt shown in Figure 3.30. In this case, two 100 pF capacitors shunt high frequency currents which
cannot flow through the bridging inductor\textsuperscript{38}. A measure of its frequency response is shown in Figure 3.31. Resonance effects can again be seen. The simulated ripple voltages at the QFN lead, while the PA is saturated, are shown in Figure 3.32.

\textbf{Figure 3.29} Schematic showing power decoupling network of driver drain supply isolated for simulation.

\textbf{Figure 3.30} PCB artwork excerpt with decoupling network highlighted.

\textbf{Figure 3.31} Response of driver Vdd decoupling network vs. frequency.

\textsuperscript{38} This inductor has an SRF under 2 GHz—it had to be replaced, as discussed in Chapter 4.
Figure 3.32 Time-domain display of simulated voltage ripple of switch Vdd supplies.

3.3.2 Gate Bias Feed Networks

All gate bias voltages are fed to the IC with series inductors. The inductor is part of a matching circuit between the gate and input balun in the first amplifier stage. The feed inductors of the second stage function as DC chokes. Three ATC600S 100 pF capacitors filter the terminal block side of these feeds. The response of the parallel capacitors themselves can be seen in Figure 3.35, having simulated the circuit of Figure 3.33 – again, resonance effects are seen. The layout of both networks is shown in Figure 3.34.

Figure 3.33 Circuit simulated to illustrate the typical response of gate-bias decoupling networks.
Figure 3.34 PCB layout excerpt with (a) switching stage, (b) driver stage gate bias circuitry highlighted.

Figure 3.35 Response of decoupling network used for gate bias supplies.
CHAPTER 4

MEASUREMENT

This final chapter focused on the power amplifier design presents its lab characterization. Section 4.1 details observed oscillations and their elimination. Section 4.2 shows a first set of measurements which were back-fit to simulation. Section 4.3 discusses tuning and measuring the design after reasonable agreement between measurements and the back-fit simulations. Finally, section 4.4 shows measurements of the bandwidth and output power spectrum of the PA. Five PAs were assembled, each is discussed as boards one through five. All simulated and measured data correspond to a 'default' bias condition unless otherwise noted: switching stage drain supply 4.7 V, driver stage drain supply 5.7 V, and gate bias supplies at -0.7 V\textsuperscript{39}. The design measured at best 57.93\% PAE (59.28\% drain efficiency), 30.5 dB linear power gain with peak output power 28.81 dBm at 930 MHz. At 1 GHz, the design measured at best 50.6\% PAE (51.26\% drain efficiency), 30.8 dB power gain, and peak output power 28.64 dBm. The measured power gain at the high-efficiency point was 16.42 and 19 dB in the two cases.

4.1 Stabilization

The test bench arranged for characterization of the design is seen in Figure 4.2. A

\textsuperscript{39} Measurements were taken with driver Vdd increased 1 V to 5.7 V from the design-phase choice because simulations performed after the design went out for fabrication showed an increase in power gain and output power on the order of 0.2 dB, with maximum PAE increasing about 1\%. Further increase would risk device damage. The two stages were measured at gate-source biases of -0.7 V, slightly lower than the design-phase simulations, by similar reasoning.
schematic and description of the setup is presented in Section 4.2 after the discussion of stability problems here. Beginning with board two, oscillations at 12 MHz and its harmonics were observed. Initially, the board was arranged to measure small-signal gain and verify the assembly but significant power readings were seen with the RF input off\(^\text{40}\). A high-frequency oscilloscope was used to observe energy flowing out of both ports of the PA\(^\text{41}\). The source was isolated to the second amplifier stage by putting that stage into cut-off to observe no oscillations. Likewise, leaving the driver stage cut off with the switching stage on started the oscillations. It was reasoned that the issue was insufficient low-frequency decoupling capacitance with mixing at the output stage creating harmonics. The problem was next replicated and solved on board three.

A 100 nF capacitor was added to the two drain supply nodes of the switching stage on board three. This eliminated the 12 MHz-based oscillations, 250 MHz and its harmonics now appearing. As discussed in Chapter 2, these oscillations could have been predicted but that instability (of the second stage source termination) was not seen in the simulated results until reviewed after the lab work\(^\text{42}\). Using the high-impedance probe of a low-frequency oscilloscope to lightly load various points on the board, it was seen that the oscillations were sensitive to loading the gate bias networks of the second stage\(^\text{43}\). To experiment with lowering the impedance from the package leads to ground

\(^{40}\) The power meter is an Agilent E4419B model with E4413A heads.

\(^{41}\) A Tektronix DPO71254B.

\(^{42}\) It was thought to be another decoupling problem, but adding 100 nF to the switching stage gate bias and driver stage drain supply, with 10 nF more on the switching stage gate bias and drain supply, did not solve the problem.

\(^{43}\) That probe is specified to present 13 pF between its signal and ground leads. This is a risky endeavor. It necessarily breaks the circuit symmetry, and it is possible that it could destabilize an otherwise stable part of the circuit.
there, the 100 nH feed inductors were replaced with 9.1 nH. The 250 MHz-based oscillations were eliminated, but more (which were isolated to the driver stage) now appeared at 1 GHz and its harmonics\textsuperscript{44}. Significant 300 kHz voltage ripple at \textit{all eight} bias decoupling networks was also seen on the oscilloscope – another low-frequency decoupling problem. A 1 uF capacitor added to each supply node removed the 300 kHz ripple. With the driver off, the switching stage then showed a 6 GHz oscillation, while the 1 GHz driver oscillation showed sensitivity to probing at the driver gate bias network. Board three then failed and testing continued on board four (microscopy of the die on board three showed a melted switching transistor).

Board four showed similar oscillations at 12 MHz and its harmonics, as well as replicating those seen prior after the decoupling was improved: 225 MHz with harmonics generated by the second stage, and 1.1 GHz generated by the driver stage\textsuperscript{45}. Focusing on the 1.1 GHz oscillation, it was decided that the simplest approach was experimentation with added losses. Since it is critical that the efficiency and power gain of the PA not be ruined, a first test was swapping the gate bias choke inductors in the first stage with 1.2 kOhm resistors. This removed the 1.1 GHz oscillation. Before doing the same with the second stage, the 100 nH inductors feeding the switch gates were swapped for a lower value to replicate the oscillation found on board three – 18 nH was used, which resulted in a second stage oscillation at 6.4 GHz replacing the 225 MHz-based oscillations. Replacing these inductors with 1.2 kOhm resistors removed the 6.4 GHz oscillation, fully

\textsuperscript{44} These oscillations may have previously been present (1 GHz is a multiple of 250 MHz – the two could coexist without being differentiated on the oscilloscope FFT when both stages were on).

\textsuperscript{45} More evidence that these oscillations probably co-existed during the work with board three.
stabilizing the PA. The final set of alterations is seen in Figure 4.1. With board one (tested after boards two through four) the 10 nF capacitors on switching stage Vdd were mistakenly skipped, resulting in a 6.8 GHz oscillation. With the 10 nF’s in place, the oscillation was removed. It is likely critical that every one of the modifications discussed here be in place for stability.
4.2 First Measurement Set

Simulated predictions, updated after stabilization, are compared to one another in Appendix F. The following sub-sections compare those results to measurement, describing first the calibration of the measurement setup.
4.2.1 Calibration

A block diagram of the measurement setup is shown in Figure 4.3. The signal flowing from the RF generator is split before arriving at the PA at point B. The other leg, arriving at the power meter head at point A from a 10 dB attenuator\textsuperscript{47} is measured with Channel A of the power meter. The amplified signal leaving the PA sees a 20 dB attenuator before arriving at point D (Channel B of the meter). The power meter was re-zeroed and re-calibrated before each set of measurements.

![Block diagram of measurement setup](image)

**Figure 4.3** Block diagram of measurement setup.

To find the power available to the PA during measurement, the difference in power flowing to points A and B with B terminated in 50 Ohms was added to the reading on Channel A (it was 10.2 dB)\textsuperscript{48}. The loss between the PA output, shown at point C in Figure 4.3, and the power sensor head (point D), is accounted for in calculating the power flowing out of the PA. The insertion loss of that section was

---

\textsuperscript{47} The 10 dB attenuator keeps the upper end of the intended sweep (20 dBm available to the PA) from getting close to the 20 dBm limit of the sensor head.

\textsuperscript{48} The 3 dB splitter has a nominal isolation between its outputs of 16 dB at 1 GHz – energy reflecting back from the PA input, which itself is predicted to be well matched, should not disturb the power measurement on Channel A in a significant way.
measured at 20.25 dB at 1 GHz with a network analyzer.

The DC connection to each desktop supply is shown in Figure 4.4, which shows the switching stage connection. Each stage has a drain and gate bias supply distributed to the terminal blocks of each half-circuit – in total, four supplies are used. Considerable DC current flows to the second stage (which varies with the RF drive power). The DC resistance between the second stage drain supply and board is taken into account: at the desired bias point, with the RF off, the supply was set to give 4.7 V within 10 mV at the decoupling networks. The resistance between the supply and board was calculated using the measured voltage drop between the supply and board with a current reading from the supply\(^49\). Throughout the trials, the DC power flowing to the second stage is derived accounting for this loss\(^50\).

---

\(^{49}\) 0.7 Ohms between each Vdd,sw decoupling network and desktop supply, due to the transition through alligator clips to thin copper wire before the terminal blocks.

\(^{50}\) This is not done with the driver stage DC measurements, since the current flow to the board there is small (under 15 mA) – there is very little voltage drop – and it varies only a few mA throughout the RF power sweep.
4.2.2 First Results

Three boards (boards one, three, and four) were measured before early conclusions could be drawn. Results are presented in Figures 4.5 through 4.7. The simulated data using the Angelov model, which agreed better with measurement, is presented alongside the measured data in 1 dBm increments of input power. The measured data, plotted with larger symbols, was taken in 1 dBm increments set at the RF generator. Both simulation results are included in the plots of DC behavior. Board one was measured at a few disparate points before failing. Absence of the fan assembly directing air parallel to the plane of the board, part of which can be seen at right in Figure 4.2, was found to degrade the power gain 1 to 2 dB. One transistor switch on board three leaked drain-source current when biased in cut-off with significant temperature dependence, calling into question the behavior of that board. Maximum drain efficiency, output power, and power gain of these PAs are tabulated in Table 4.1 below.

<table>
<thead>
<tr>
<th>Board Number</th>
<th>Max. Drain Efficiency(%)</th>
<th>Max. Output Power (dBm)</th>
<th>Max. Power Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>39.67</td>
<td>28.602</td>
<td>23.737</td>
</tr>
<tr>
<td>3</td>
<td>36.37</td>
<td>28.254</td>
<td>23.670</td>
</tr>
<tr>
<td>4</td>
<td>47.31</td>
<td>27.817</td>
<td>21.049</td>
</tr>
<tr>
<td></td>
<td>68.1</td>
<td>30.09</td>
<td>27.998</td>
</tr>
<tr>
<td></td>
<td>60.3</td>
<td>30.093</td>
<td>27.877</td>
</tr>
</tbody>
</table>

Table 4.1 Metrics of interest of three PA boards shown with simulated expectations.

51 The broken die on board three was replaced.
52 When probed with a multimeter at a second stage drain supply decoupling node. The boards were first checked at roughly these points to check the power gain and saturated power before the full sweep.
53 Later testing, detailed in Section 4.3, employed both this fan and a heat sink.
The following observations and conclusions were taken from the data:

- Each board showed lower power gain, efficiency, and output power than expected.
- All three boards show a saturated output power maximum within 2.3 dBm of simulation. Maximum power gain is about 4.5 to 7 dB less than simulation.
- Boards one and three match one another fairly well, showing similar efficiency, power gain, and saturated output power. Therefore, board one may have had the same leakage problem as board three (but it was not observed before that die failed). Board four was thought to be an outlier at this point in the study.
- The DC consumption of both amplifier stages is somewhat close to expectations when the input power is low on each board\(^4\). The bulk of the gain discrepancy is therefore likely due to networks external to the die, since fairly accurate prediction of gain follows from fairly accurate prediction of the bias point.
- The maximum output power is an indicator of losses between the switching devices and the load since far beyond P1DB losses on the input side of the PA are irrelevant. Therefore, some facet of the circuit at the output probably accounts for a portion of the lacking power gain on the order of the 1.2 to 2.3 dB (the difference between the measured and simulated maximum output power). Some facet of the input network probably accounts for the remaining 2.2 to 5.8 dB of 'missing' power gain.

With these points as consideration, the input and output network designs were investigated. A major flaw of omission in the simulations was then found: important sections of the PCB metal external to the packaged IC were not modeled in the design phase of the project. The following section describes that investigation.

---

\(^4\) The bias power consumed by the very large pHEMT switches is necessarily very sensitive to the gate bias used: a 10 mV increase in gate bias corresponds to roughly a 100 mW change in bias power, for instance, and no active bias circuit was included in the design.
Figure 4.5 Comparison of board four measurements with simulation. Power gain, output power, and efficiency against input power (a) shown with Angelov model simulated results, (b) DC consumption of both amplifier stages shown with simulation results using both models.
Figure 4.6 Comparison of board three measurements with simulation. Power gain, output power, and efficiency against input power (a) shown with Angelov model simulated results, (b) DC consumption of both amplifier stages shown with simulation results using both models.
Figure 4.7 Comparison of board one measurements with simulation. Power gain, output power, and efficiency against input power (a) shown with Angelov model simulated results, (b) DC consumption of both amplifier stages shown with simulation results using both models.

4.2.3 Refined Simulation Results

The following omitted features were found to have significant effects on the performance of the simulated PA:
• the wide copper traces between the driver stage drain supply decoupling capacitors and the QFN package, e.g. Figure 4.8.
• the microstrip between the input SMA jack and the differential inputs to the QFN package, e.g. Figure 4.9.
• the microstrip lines between the output balun and output SMA jack, e.g. Figure 4.9.

The wide metal traces of Figure 4.8 and curved sections of of Figure 4.9 were modeled with the 2D FEM solver available in ADS\textsuperscript{55}. Schematic-level transmission line models were used for the remaining microstrip. Table 4.2 shows chronologically by row the changes in simulated performance as alterations were made. The bias currents of the two stages were matched within 1 mA of measurements on boards one and three by adjusting the simulated gate-source bias voltages first\textsuperscript{56}. The switching stage was biased to -0.69 V with drivers at -0.75 V for the Angelov model. With the Parker-Skellern model, -0.68 V and -0.75 V were simulated.

\textbf{Figure 4.8} Metal of driver stage decoupling networks (yellow) which were added to simulation.

\textsuperscript{55} With the same board stack-up as the 3D models of Chapter 3: 1 oz. copper on 31-mils thick RT/Duroid 5880.

\textsuperscript{56} There is natural variation to the DC and RF transconductance of active devices of a given process. This does not capture that effect exactly, but helps model the results seen in measurement with what is available to adjust in simulation.
Figure 4.9 PCB artwork excerpts displaying microstrip sections of the input network (left) and output network (right) whose models were added to simulations after first measurements.

<table>
<thead>
<tr>
<th>Alteration to Simulation</th>
<th>Max. Drain Efficiency(%)</th>
<th>Max. Output Power (dBm)</th>
<th>Max. Power Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Before Measurement</td>
<td>68.1</td>
<td>30.09</td>
<td>27.998</td>
</tr>
<tr>
<td>Match Measured DC Bias</td>
<td>67.7</td>
<td>30.114</td>
<td>27.844</td>
</tr>
<tr>
<td>Add Driver Decoupling Shape</td>
<td>62.5</td>
<td>29.966</td>
<td>22.781</td>
</tr>
<tr>
<td>Add Input Microstrip</td>
<td>62.5</td>
<td>29.99</td>
<td>25.727</td>
</tr>
<tr>
<td>Add Output Microstrip</td>
<td>54.1</td>
<td>28.556</td>
<td>24.877</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Alteration to Simulation</th>
<th>Max. Drain Efficiency(%)</th>
<th>Max. Output Power (dBm)</th>
<th>Max. Power Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Before Measurement</td>
<td>60.3</td>
<td>30.093</td>
<td>27.877</td>
</tr>
<tr>
<td>Match Measured DC Bias</td>
<td>60.2</td>
<td>30.079</td>
<td>27.406</td>
</tr>
<tr>
<td>Add Driver Decoupling Shape</td>
<td>57.3</td>
<td>30.299</td>
<td>21.784</td>
</tr>
<tr>
<td>Add Input Microstrip</td>
<td>58.3</td>
<td>30.325</td>
<td>24.727</td>
</tr>
<tr>
<td>Add Output Microstrip</td>
<td>50.3</td>
<td>28.856</td>
<td>23.951</td>
</tr>
</tbody>
</table>

Table 4.2 Effect of successively refining simulation with board features critical to PA performance.
Modeling the microstrip at the amplifier output shows a cost of approximately 1.4 dB saturated output power and 0.8 dB power gain with either of the device models. This confirms the suspicion of a roughly 1.2 dB loss there. Modeling the driver stage decoupling metal is significant: a decrease to maximum gain of roughly 5 to 5.6 dB results with both models, matching the earlier suspicion as well\(^7\). Modeling the microstrip between the elements of the input network has increased the peak power gain of the simulated PA by just under 3 dB with both models, now matching measurements on two of three boards (boards one and three) more closely, c.f. Table 4.3. Both simulations show higher peak power gain than measured, with the Parker-Skellern-based simulation disagreeing with measurement more than 25% (more than 1 dB) for the two boards – the Angelov-based simulation agrees with both boards within 6.3%. The simulations disagree with the peak output power measured on board one by 1.06% and 5.66% using the Parker-Skellern and Angelov models, respectively. For board three, the disagreement is 6.71% and 12.92%.

<table>
<thead>
<tr>
<th>Board Number</th>
<th>Max. Drain Efficiency(%)</th>
<th>Max. Output Power (dBm)</th>
<th>Max. Power Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>39.67</td>
<td>28.602</td>
<td>23.737</td>
</tr>
<tr>
<td>3</td>
<td>36.37</td>
<td>28.254</td>
<td>23.670</td>
</tr>
<tr>
<td></td>
<td>54.1</td>
<td>28.556</td>
<td>24.877</td>
</tr>
<tr>
<td></td>
<td>50.3</td>
<td>28.856</td>
<td>23.951</td>
</tr>
</tbody>
</table>

**Table 4.3** Metrics of interest measured with PA boards one and three with refined expectations.

\(^7\) It is interesting that with this change the output power is increased more than 5% in the Angelov case, and the output power drops more than 3% in the Parker-Skellern case. Since the peak power gain has dropped by similar amounts in both cases, this is likely an indication that there is a significant difference between the non-linear response of the two models to altering the source terminations of the switching stage.
The full power sweep curves of these two refined simulations are compared in section two of Appendix F: one conspicuous change from prior simulated expectations being the similar DC behavior between the two models in the switching regime c.f. Figure 4.5(b), Figure F.2.2. The simulations are compared to the first round of measurements in Figures 4.10 through 4.12. The following observations and conclusions were taken from the refined simulation study:

- The refined simulations match in form the DC behavior of board four, that board which was prior thought to be an outlier due to low gain and output power. That behavior, where DC power decreases with increasing input power, is the expected behavior of a switching PA.
- Boards one and three showed the opposite, with DC power increasing in the switching regime, but these results are close to the refined expectations otherwise. The DC leakage seen on board three with the switches held in cut-off, which appeared on the order of 75 mA, is then probably related to the behavior of that board at high input powers. Board one likely had this problem as well.
- With the prior two points as consideration, replacing the die on board one or three would likely show a peak drain efficiency closer to the 50-54% range now simulated. Similar to board four, the DC behavior would likely match the simulations more closely with either of the two models after replacing these die.

These assertions were tested in the next rounds of study, in parallel with work discussed in Section 4.3 toward optimizing the input and output matching networks for more output power and gain, though it will be seen that the third point was not perfectly clear after testing with die from a second wafer. The interested reader is directed to section three of Appendix F for a short variation study of the output balun and VSWR at the output SMA connector. It shows the measured results of boards one and three within a set of likely design outcomes.

58 As the swings across the gate-source junctions of the switches increase, the switches are farther and farther cut off for roughly half of the RF cycle while the drain-source voltages swing high.
Figure 4.10 Comparison of board four measurements with refined simulation. Power gain, output power, and efficiency against input power (a) shown with Angelov model simulated results, (b) DC consumption of both amplifier stages shown with simulation results using both models.
Figure 4.11 Comparison of board three measurements with refined simulation. Power gain, output power, and efficiency against input power (a) shown with Angelov model simulated results, (b) DC consumption of both amplifier stages shown with simulation results using both models.
Figure 4.12 Comparison of board one measurements with refined simulation. Power gain, output power, and efficiency against input power (a) shown with Angelov model simulated results, (b) DC consumption of both amplifier stages shown with simulation results using both models.

4.3 Second Measurement Set

The input and output networks of the PA were tuned after the back-fitting described in the prior section. Section 4.3.1 shows the retuning method and results on
board three. Boards whose die were damaged (boards one and four\textsuperscript{59}) were re-worked with fresh die before tuning them – those final results are presented in Section 4.3.2.

4.3.1 Retuned Input/Output Sections

With the back-fit agreeing reasonably well with measurement, source and load pulls were simulated to find desirable reflection coefficients looking 'out' from the baluns (looking at the signal source and the load). For the input balun, the source was set to -25 dBm to study gain circles. For the output balun, the PA was simulated in saturation at 12 dBm input power to study output power and efficiency circles. Schematic models of the terminations before tuning are shown in Figure 4.13 and 4.14. Comparison to the circles is seen in Figure 4.15 and Figure 4.16. The 'after' reflection coefficients correspond to the redesigned networks of Figure 4.17. Improvement was first demonstrated on board three with these networks\textsuperscript{60}.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure4.13}
\caption{Simulation of input balun single-ended termination before alteration.}
\end{figure}

\textsuperscript{59} Board four failed when experimenting with increased switching stage DC supply voltages.
\textsuperscript{60} The topology of these networks was found simply by trial and error in simulation with solder-able alterations in mind. The value of each element was chosen by iteration.
The new input network simulates approximately 4 of the 5 dB possible improvement in linear power gain. The new output network simulates approximately 4 percentage points more PAE with a 1 dB increase in maximum output power\textsuperscript{61}. The effect of each is shown by row in Table 4.4. The alterations to board three can be seen in Figures 4.18 and 4.19.

\textbf{Figure 4.15} Simulated source pull results showing input balun terminations for linear power gain.

\textsuperscript{61} It is interesting that the optimum termination for PAE is not coincident with the optimum termination for output power. It is likely that the peak output power occurs near the reflection coefficient which best matches to the output balun, which is not guaranteed to be the optimum for return loss from the perspective of the switches (or for their harmonic terminations).
Figure 4.16 Simulated load pull showing output balun terminations for PAE and output power (dBm).

Figure 4.17 Altered input (top) and output (bottom) networks.
<table>
<thead>
<tr>
<th>Alteration to Simulation</th>
<th>Max. Drain Efficiency(%)</th>
<th>Max. Output Power (dBm)</th>
<th>Max. Power Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Parker-Skellern</td>
</tr>
<tr>
<td>Schematic Refined</td>
<td>54.1</td>
<td>28.556</td>
<td>24.877</td>
</tr>
<tr>
<td>Change Input Network</td>
<td>53.9</td>
<td>28.555</td>
<td>29.604</td>
</tr>
<tr>
<td>Change Output Network</td>
<td>57.9</td>
<td>29.472</td>
<td>30.166</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Angelov</td>
</tr>
<tr>
<td>Schematic Refined</td>
<td>50.3</td>
<td>28.856</td>
<td>23.951</td>
</tr>
<tr>
<td>Change Input Network</td>
<td>50.2</td>
<td>28.853</td>
<td>28.75</td>
</tr>
<tr>
<td>Change Output Network</td>
<td>54.2</td>
<td>29.831</td>
<td>29.224</td>
</tr>
</tbody>
</table>

Table 4.4 Effect of successive revisions to the input and output networks in simulation.

Figure 4.18 Altered input network seen on board three.
Figure 4.19 Altered output network seen on board three.

Measured results from board three are presented in Figure 4.20. Simulated expectations can be seen in full in section four of Appendix F: roughly 200 mW more DC power flows to the second stage in the switching regime. This implies that tuning at the load side of the output balun has disturbed the harmonic terminations of the PA while improving the fundamental match (overall, the output power and efficiency have increased). Finally, metrics of interest are tabulated with prior measurement results in Table 4.5.
Figure 4.20 Comparison of measured board three, with alterations, to simulated expectations. Power gain, output power, and efficiency against input power (a) shown with Angelov model simulated results, (b) DC consumption of both amplifier stages shown with simulation results using both models.

### Table 4.5
Measured results before/after alterations on board three shown with simulated expectations.

<table>
<thead>
<tr>
<th>Board State</th>
<th>Max. Drain Efficiency (%)</th>
<th>Max. Output Power (dBm)</th>
<th>Max. Power Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Before</td>
<td>36.37</td>
<td>28.254</td>
<td>23.670</td>
</tr>
<tr>
<td>After</td>
<td>42.72</td>
<td>28.945</td>
<td>29.087</td>
</tr>
<tr>
<td></td>
<td>57.9</td>
<td>29.472</td>
<td>30.166</td>
</tr>
<tr>
<td></td>
<td>54.2</td>
<td>29.831</td>
<td>29.224</td>
</tr>
</tbody>
</table>

Measured Output Power, Power Gain, Drain Efficiency, and Power-Added Efficiency vs. Available Input Power
Board #3 with Input/Output Network Alterations Compared to Simulation (Angelov)

Measured DC Power vs. Available Input Power
Board #3 with Input/Output Network Alterations Compared to Simulations
It is seen in Table 4.5 that the alterations have improved the PA performance: the maximum output power has increased by 0.69 dBm, the maximum power gain has increased 5.4 dB, and the drain efficiency of the PA has increased by 6.35 percentage points where the expected increases, discussed in the prior section, were approximately 0.9 dBm, 5.2 dB, and 4 percentage points. The drain efficiency is still low, likely due to the leakage problem, and the simulations still overestimate the power gain and peak output power.

### 4.3.2 Results with Replaced Die

The tuned design was next studied on boards one and four with fresh die from a second wafer. The measurement setup was altered to better take advantage of the thermal vias under the IC: a commercial heat sink assembly was placed beneath the boards, seen in Figure 4.21\(^6\). The heat pipes feed a fin and fan assembly with air blowing parallel to the plane of the board. The interface between the board and heat piping was coated with non-adhesive thermal compound.

The board four results are shown in Figure 4.22 and recorded in Table 4.6 with the results of board one (which are shown in full in Figure 4.23). These measurements could not be reconciled with simulation by perturbing simulated bias voltages to match the DC behavior as done previously. The dataset compared to measurement in Figures 4.22 and 4.23 is the same as that which was compared to board three in the last section.

---

6\(^2\) The “Coolermaster Hyper 101”, which was available at a local consumer electronics vendor. The heat sink includes a DC-controlled fan which was operated off a 24 V DC supply on the test bench.
The DC consumption of the new die is lower than expected while their RF transconductance appears to be equal if not higher than the first set of die.

![Photograph of second experimental setup and heat sink interface.](image)

**Figure 4.21** Photograph of second experimental setup and heat sink interface.

<table>
<thead>
<tr>
<th>Board Number</th>
<th>Max. Drain Efficiency(%)</th>
<th>Max. Output Power (dBm)</th>
<th>Max. Power Gain (dB)</th>
<th>Simulated expectations</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>51.26</td>
<td>28.64</td>
<td>30.881</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>47.94</td>
<td>27.75</td>
<td>30.191</td>
<td></td>
</tr>
<tr>
<td></td>
<td>57.9</td>
<td>29.472</td>
<td>30.166</td>
<td>Simulated (Parker-Skellern)</td>
</tr>
<tr>
<td>5</td>
<td>54.2</td>
<td>29.831</td>
<td>29.224</td>
<td>Simulated (Angelov)</td>
</tr>
</tbody>
</table>

**Table 4.6** Measured results after input/output network alterations and new die on boards one and four shown with simulated expectations.
Figure 4.22 Comparison of measured performance of board four, with new die and alterations, to simulated expectations. Power gain, output power, and efficiency against input power (a) shown with Angelov model simulated results, (b) DC consumption of both amplifier stages shown with simulation results using both models.

The results measured with board one provide further evidence that leakage was likely present with the prior die. The maximum drain efficiency has increased nearly 12%
with near-equal maximum output power. The output power did not increase as expected per the tuned matching networks, despite increased gain, most likely because of the reduced DC conductance of the devices from the second wafer (there was simply less DC power absorbed by the second stage to be converted to RF).

Since the simulation could not be brought in line with measurement, board one was again measured with the bias power of the switching stage increased toward that simulated by bringing the gate-source bias up by 40 mV. Results with that experiment, shown in Figure 4.11, are slightly degraded, showing peak drain efficiency 50.28%, peak output power 28.81 dBm with power gain of 30.28 dB. Interestingly, the switching stage DC behavior agrees with the Parker-Skellern model at high powers. A further modification to the setup was made in order to demonstrate 1 Watt of output power: the drain supply of the switching stage was increased to 5.7 V with the gate-bias left at -0.66 V. Measured results showing peak output power 30.08 dBm, maximum gain 29.772 dB, peak drain efficiency 48.95%, and maximum power-added efficiency 48.45% are seen in Figure 4.12. The diminished linear gain and efficiency in these two trials, in comparison to the original 4.7 V/-0.7 V bias condition, may be due to heating.

---

63 Prior output power measurements were about 1.2 dBm below 30 dBm (1 W). The output power of the CMCD stage in theory goes as $V_{dd,sw}^2$, which implies a supply voltage increase by a scalar factor of 1.2 to 5.7 V.
Comparison of measured performance of board one, with new die and alterations, to simulated expectations. Power gain, output power, and efficiency against input power (a) shown with Angelov model simulated results, (b) DC consumption of both amplifier stages shown with simulation results using both models.
Figure 4.24 Performance of board one, with new die and alterations, and switching stage gate bias voltage increased. Power gain, output power, and efficiency against input power (a), (b) DC consumption of both amplifier stages shown with simulation results using both models.
Figure 4.25 Performance of board one, with new die, alterations and bias supplies adjusted to achieve 1 Watt output power. Power gain, output power, and efficiency against input power (a), (b) DC consumption of both amplifier stages.

4.4 Bandwidth and Spectrum Measurements

Final tests of the PA design include measurement of the bandwidth over which it
operates at highest efficiency and output power, as well as the spectrum of the output. It was verified that the signal is not significantly distorted, and that it exhibits best efficiency in the range of 930 to 960 MHz. The attentive reader will recall that the FEM study of the harmonic termination network, presented in Chapter 3, concluded with a third harmonic termination detuned to approximately 100 MHz below the 3 GHz target. Peak measured performance from 930 to 960 MHz is telling, since the third harmonic in this band falls only 20 to 110 MHz below the 'best harmonic short' frequency per those FEM results. Part variation, especially in the hand-wound transmission line balun, likely plays a role in detuning the terminations as well\textsuperscript{64}. The output power was measured nearly constant over a larger bandwidth, about 930 MHz to 1.03 GHz.

4.4.1 Bandwidth

The bandwidth of the amplifier was measured at the drive level of the peak efficiency point from the prior 1 GHz measurements (9.3 dBm drive power for board three, 10 dBm for board one). The drive frequency was varied in steps of 10 MHz with areas of interest oversampled. Figures 4.26 and 4.27 show the measured data with simulated results using 10 dBm input power. Board three reaches maximum 43.28% drain efficiency (42.84% PAE) and board one reaches 58.06% drain efficiency (57.487% PAE). Both boards achieve saturated powers within 1 dB of their maxima in a roughly 130 MHz-wide band centered around 975 MHz. They achieve efficiencies within 10% of

\textsuperscript{64} The transmission lines formed by the twisted pairs wound on the ferrite are very hard to manufacture consistently by hand since interwinding capacitance and loop inductance is hard to control, while the ferrite core itself will deliver some range of permeabilities supporting the lines.

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their maxima there. If one takes a tighter view, in which efficiency is within 2% of maximum, for example, this is achieved in a 50 MHz bandwidth around roughly 930 to 950 MHz center frequency.

![Measured Saturated Output Power vs. Frequency Boards One and Three with Simulated Results](image)

**Figure 4.26** Saturated output power against frequency for boards one and three, shown with simulation.

![Measured Drain Efficiency and Power-Added Efficiency vs. Frequency Boards One and Three Shown with Simulation Results](image)

**Figure 4.27** Drain efficiency and power-added efficiency against frequency for boards one and three, shown with simulation.

A final power sweep with board one, at 930 MHz, the frequency at which its measured efficiency maximized, is shown in Figure 4.28. Peak drain efficiency was 59.28%, with 57.93% PAE, 30.5 dB linear gain and peak output power 28.81 dBm. This is the best measured performance of the design.
Figure 4.28 Performance of board one, with new die and alterations, at 930 MHz. Power gain, output power, and efficiency against input power (a), (b) DC consumption of both amplifier stages.

4.4.2 Spectrum

The spectral content of the PA output was observed on boards one and three (the best and worst cases of the entire study) with a real-time FFT from a Tektronix
DPO71254B oscilloscope. The spectrum with board one operating in the switching regime is seen in Figure 4.29, where it is driven with 10 dBm input power at 1 GHz. The second harmonic dominates, but is still more than 26 dB down from the fundamental – surprisingly high. Considerable even-harmonic power is indicative of an imbalance between the two half-circuits of the PA, which could be investigated starting at the hand-wound baluns. The third harmonic is more than 47 dB down from the fundamental.

Taking the sum of power in the harmonics, the measurements from board one at 1 GHz, which were taken by power meter (recording total power seen by its sensor head), can be said to be overestimated by roughly 0.23% for high input powers. With board three the third harmonic was only 10.8 dB down with second harmonic power 39.6 dB down. Therefore, the measured results with board three are overestimated roughly 8.4% at high powers.

![Power spectrum](image)

**Figure 4.29** Power spectrum of board one output with PA operating in the switching regime (10 dBm input power). Markers placed at 1 GHz and 2 GHz peaks illustrate 2nd harmonic distortion 26.4 dB down.
CHAPTER 5

IMAGE-REJECT POWER MIXER

This chapter details a secondary goal of this thesis: to document research into the use of the CMCD as a sub-circuit in a power mixer. Section 5.1 provides an overview of the mixer topology and its potential applications. Section 5.2 reviews conversion matrix analysis and documents its application to the mixer circuit (Appendix G provides detail). Finally, section 5.3 discusses the practicality of the circuit, which was not developed into a prototype.

5.1 Overview

The mixer topology, shown simplified in Figure 5.1, unites the up-conversion mixer and power amplifier circuits typically separate in wireless transmitters, similar to work by Kousai and Hajimiri [62]. Their CMOS transmitter delivered over one Watt of RF power by summing currents from an array of transconductance mixers, each mixer being turned on and off dynamically in order to minimize power consumption and maintain linearity. The topology of Figure 5.1 can be seen as four CMCD PAs combining power in a shared secondary loop. The PA switches behave as passive mixers in which intermediate frequency (IF) signals provide supply modulation while local oscillators (LOs) drive the device gates. The switches constitute time-varying conductances which up-convert DC and IF voltages to high-frequency currents coupling into the secondary: a
CMCD PA with modulation is an up-conversion mixer.

The right half-circuit of Figure 5.1 negates the currents flowing to the load from the left half-circuit at the image frequency, while the bottom half-circuit nullifies the local oscillator feed-through currents of the top half (those which are due to up-conversion of the DC bias at the device drains). In this way, an image-reject 'power mixer' is realized, possibly appropriate for quadrature amplitude modulation (QAM) systems.

![Simplified schematic of the image-reject power mixer with antenna load](image)

**Figure 5.1** Simplified schematic of the image-reject power mixer with antenna load $Z_L$ shown at bottom, information being encoded by $v_i(t), q(t)$ for $v_i = v_i(t)\cos(\omega_{if} t + q(t))$, $v_q = -v_i(t)\sin(\omega_{if} t + q(t))$. The left half-circuit LO is driven by $\cos(\omega_{lo} t)$, while $\sin(\omega_{lo} t)$ is used at right.

An additional concept investigated in this chapter was inspired by the work of Andrews and Molnar. In 2010, they showed that the impedance looking into the IF port
of a quadrature passive mixer is a discernible function of the load impedance at the RF port and vice versa, a property they called 'passive mixer transparency' [63,64]. In their work, which focused on adaptive noise figure minimization in software-defined radios\(^65\), a feedback circuit mixed in-phase and quadrature currents at the inputs of two baseband amplifiers in a receiver without a low-noise amplifier (LNA). A block diagram of their 'mixer-first', LNA-less receiver is shown in Figure 5.2: the quadrature baseband currents mix before the amplifiers subject to variable resistive feedback, thereby controlling the impedance loading the mixers' IF ports and altering the impedance presented to the antenna at the RF frequency by transparency.

![Figure 5.2](image)

**Figure 5.2** (a) Schematic of proposed LNA-less receiver by Andrews and Molnar. (b) Software-controlled feedback connections, shown by dotted lines, which manipulate the IF loads of the mixers in the design [64].

In contrast, the power mixer of Figure 5.1 is targeted for passive-mixer *transmitters* in which the IF drivers would provide the power instead of an RF PA. RF currents flowing

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\(^65\) Software-defined radios are transceivers in which system blocks (mixers, amplifiers, filters, etc.) are realized with software that processes digitized signals and/or controls extant hardware. They are often designed to reconfigure, changing carrier frequency and even signal formats – thus, dynamic tuning of antenna mismatches is a priority.
in the shared secondary loop reflect to the primaries of the four transformers where they are down-converted to IF by the switching devices, thereby altering the impedance presented to the IF drivers – an example of passive mixer transparency. This ability to translate the antenna impedance to the IF ports is also a mechanism for tuning out antenna mismatches by translating a variable IF impedance in the opposite direction. This concept was investigated using conversion matrix techniques and harmonic balance simulation [65]. However, evolving from schematic-level simulation to hardware demonstration proved to be a problem: available balun transformers appropriate for a design at L-band seem to disturb the terminating conditions of the mixer-amplifiers. That is, simulations and analysis using ideal transformers, which showed mixer transparency, were not developed into a feasible, efficient design.

5.2 Conversion Matrix Analysis

This section describes the conversion matrix analysis of the mixer. Following the introduction of section 5.2.1, the conversion matrix of a single transistor switch is derived in terms of device parameters in section 5.2.2. An envelope-modulated CMCD is analyzed as a passive mixer in section 5.2.3. Finally, the conversion matrix treatment of the image-reject CMCD power mixer is presented in section 5.2.4.

5.2.1 Introduction

Non-linear elements can be analyzed with conversion matrices which relate their
responses at several frequencies. In addition, the technique can extend nodal and mesh analysis, since it is a linearization of a non-linear problem. To motivate the analysis of the power mixer, the technique, described in [65], is repeated here with a derivation of the conversion matrix of a pHEMT switch and the transparency analysis of a modulated current-mode class-D (CMCD) power amplifier.

The terminal current of a non-linear resistance, an example of which is seen in Figure 5.3, is some non-linear function \( f(V) \) of its terminal voltage. Assuming voltage \( V(t) \) to be comprised of some large-signal \( V_o(t) \) and a small-signal variation \( v(t) \), a situation of interest in resistive mixing applications, the current response may be expanded in a Taylor series analogous to linear small-signal analyses:

\[
I = f(V_0 + v) = f(V_0) + \frac{d}{dV} f(V)_{V=V_0} \cdot v + \frac{1}{2} \frac{d^2}{dV^2} f(V)_{V=V_0} \cdot v^2 + \frac{1}{6} \frac{d^3}{dV^3} f(V)_{V=V_0} \cdot v^3 + \ldots
\]

where the linear response to signal \( v \) may be found by subtracting the large-signal component of the current from the total current \( I \) under the assumption that the terms non-linear in \( v(t) \) are negligible:

\[
i(v) = I(V_0 + v) - I(V_0)
\]

The small signal current \( i(v) \) can be expressed over time in terms of a *time-varying conductance* \( g(t) \) as:

\[
i(t) = \frac{d}{dV} f(V)_{V=V_o(t)} \cdot v(t) = g(t) \cdot v(t)
\]

where \( V_o(t) \) is an arbitrary large-signal voltage.
It is seen that the time-varying conductance is the derivative of the I/V characteristic of the non-linear resistance at the time-varying, large-signal control voltage. If the non-linear element has two or more controlling large-signal voltages, additional conductances may be derived from a Taylor expansion in additional dimensions. For example, in the case of the output conductance of a switching FET it is necessary to incorporate transconductance effects by expanding \( I_{DS} = f(V_{GS}(t), V_{DS}(t)) \) to extract the small-signal drain current component \( i_{ds}(t) = g_m(t) \cdot v_{gs}(t) + g_{ds}(t) \cdot v_{ds}(t) \) and time-varying conductances \( g_m(t) \) and \( g_{ds}(t) \) as:

\[
g_m(t) = \left. \frac{d}{dV_{GS}} f(V_{GS}(t), V_{DS}(t)) \right|_{V_{gs} = v_{gs}(t)}^{V_{gs} = V_{gs}(t)}
\]

\[
g_{ds}(t) = \left. \frac{d}{dV_{DS}} f(V_{GS}(t), V_{DS}(t)) \right|_{V_{gs} = v_{gs}(t)}^{V_{gs} = V_{gs}(t)}
\]

where \( V_{gs}(t), v_{gs}(t) \) and \( V_{ds}(t), v_{ds}(t) \) are the large and small signal components of total voltages \( V_{GS}(t) \) and \( V_{DS}(t) \), respectively.
To derive the time-varying drain-source conductance of a transistor switch used as a passive mixer, it is assumed that the gate drive is sufficient to place the device strictly in its cut-off and triode (linear resistance) regions. Such a switch is studied to illustrate the conversion matrix approach, though the topology studied in this chapter does not employ a small-signal modulating signal $v_{ds}(t)$: the power mixer analysis assumes a large drain-source signal swing throughout which the drain-source conductance is assumed to be the same as the small-signal case. Assuming first that the gate drive is a perfect square-wave with fundamental frequency $\omega_0$ having DC value $V_\beta$ and peak voltage $V_\alpha + V_\beta$, as seen in Figure 5.4, the waveform may be described by its Fourier series, for transistor threshold voltage $V_{th}$:

$$V_{GS}(t) = 4\pi V_\alpha \sum_{n=0}^{\infty} \left(\frac{1}{2n+1}\right) \cos \left(\frac{(2n+1)\omega_0 t}{2n+1}\right) + V_\beta, \quad V_\alpha + V_\beta > V_{th}, \quad V_\beta < V_{th}$$

![Figure 5.4 Ideal square-wave drive waveform for derivation of time-varying switch conductance.](image)

The conventional triode-region drain current expressions apply:

$$I_{DS}(t) = f(V_{GS}(t), V_{DS}(t)) = \begin{cases} \kappa \left( V_{GS}(t) - V_{th} \right) V_{DS}(t) - \frac{V_{DS}^2(t)}{2}, & V_{GS}(t) > V_{th} \\ 0, & V_{GS}(t) \leq V_{th} \end{cases}$$

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where \( \kappa \) accounts for sizing and process parameters. Taking \( g_{ds}(t) \) gives:

\[
g_{ds}(t) = \frac{d}{dV_{DS}} I_{DS}(t) \bigg|_{V_{GS}=V_{ds}(t)} = \begin{cases} \kappa \left( V_{GS}(t) - V_{th} \right) - V_{DS}(t) & , \quad V_{GS}(t) > V_{th} \\ 0 & , \quad V_{GS}(t) \leq V_{th} \end{cases}
\]

For a CMCD switch, the voltage across the drain-source connection of the device, \( V_{DS}(t) \), is assumed small for the half-cycle in which the switch is on (it is zero in the idealized case). In addition, \( V_{GS}(t) \) is held constant throughout each half-cycle under the assumption of square-wave drive: it reaches a peak \( V_{\alpha} + V_{\beta} \) and includes no small-signal variation. Therefore, additional simplifications may be made to \( g_{ds}(t) \) and the small-signal response \( i_{ds}(t) \):

\[
g_{ds}(t) = \begin{cases} \kappa \left( V_{\alpha} + V_{\beta} - V_{th} \right) & , \quad V_{GS}(t) > V_{th} \\ 0 & , \quad V_{GS}(t) \leq V_{th} \end{cases}
\]

\[
i_{ds}(t) = g_{m}(t) \cdot v_{gs}(t) + g_{ds}(t) \cdot v_{ds}(t) \quad , \quad v_{gs}(t) = 0 \quad \Rightarrow \quad i_{ds}(t) = g_{ds}(t) \cdot v_{ds}(t)
\]

It is seen that the time-varying conductance \( g_{ds}(t) \) of the switch follows the shape of the square-wave drive, illustrated in Figure 5.5. As previously discussed, conductance \( g_{ds}(t) \) applies to small-signal forcing of \( v_{ds}(t) \). If one takes a large-signal drain conductance \( G_{DS}(t) \) from the triode-region equations for current with the same assumptions, the result is identical:

\[
G_{DS}(t) = \frac{d}{dV_{DS}} I_{DS}(t) = \begin{cases} \kappa \left( V_{GS}(t) - V_{th} \right) - V_{DS}(t) & , \quad V_{GS}(t) > V_{th} \\ 0 & , \quad V_{GS}(t) \leq V_{th} \end{cases}
\]

\[
V_{DS}(t) \ll V_{GS}(t) - V_{th} \quad , \quad V_{GS}(t) = \begin{cases} V_{\alpha} + V_{\beta} & , \quad V_{GS}(t) > V_{th} \\ 0 & , \quad V_{GS}(t) \leq V_{th} \end{cases} \quad \Rightarrow \quad G_{DS}(t) = g_{ds}(t)
\]
However, the small-signal analysis is continued here after [65] to motivate the conversion matrix method used for the power mixer analysis.

\[ \kappa(V_\alpha + V_\beta - V_{th}) \]

\[ g_{ds}(t) \]

\[ t = 0 \quad t = 1/f_0 = 2\pi/\omega_0 \]

**Figure 5.5** Time-varying conductance waveform of a pHEMT switch with square gate drive.

The harmonic components of the drain-source conductance, seen by its square shape, give rise to frequency mixing when an intermediate-frequency (IF) signal \( v_{ds}(t) = v_{IF}\cos(\omega_{IF}t) \) is applied. The gate-source terminals are taken as the local oscillator (LO) input as in Figure 5.6.

\[ v_{ds}(t) = v_{IF}\cos(\omega_{IF}t) \]

**Figure 5.6** Illustration of pHEMT used as passive mixing switch.

This can be seen by expressing the conductance waveform by its Fourier series with the IF signal taken into consideration:
\[ g_{ds}(t) = 4 \frac{K}{\pi} (V_a + V_b - V_{th}) \sum_{n=0}^{\infty} (-1)^n \cos \left( \frac{(2n+1)\omega_{LO} t}{2n+1} \right) \frac{K}{2} (V_a + V_b - V_{th}) \]

\[ i_{ds}(t) = g_{ds}(t) v_{ds}(t) = 4 \frac{K}{\pi} (V_a + V_b - V_{th}) \left\{ \sum_{n=0}^{\infty} (-1)^n \cos \left( \frac{(2n+1)\omega_{LO} t}{2n+1} + \frac{\pi}{8} \right) \right\} v_{IF} \cos (\omega_{IF} t) \]

\[ \Rightarrow i_{ds}(t) = \frac{K v_{IF}}{2} (V_a + V_b - V_{th}) \left\{ 4 \sum_{n=0}^{\infty} (-1)^n \cos \left( \frac{(2n+1)\omega_{LO} \pm \omega_{IF} t}{2n+1} \right) + \cos (\omega_{IF} t) \right\} \]

where it is shown that the small-signal drain current response includes mixing tones around each harmonic of the LO frequency.

A frequency-domain approach relating the circuit response at all tones of interest is expedient when analyzing such a time-varying circuit element excited by two or more tones. This is the impetus for the conversion matrix method. Assuming the IF drive is a single tone at \( \omega_{IF} \), the mixing element will sustain currents and voltages at \( \omega = n \cdot \omega_{LO} \pm \omega_{IF} \) for integer \( n \). However, in a frequency-domain treatment using complex-valued phasor quantities, the notation may be simplified, since superposition applies, and positive and negative frequencies are complex conjugate pairs [65].

Therefore, the circuit response may be studied at frequencies \( \omega_n = n \cdot \omega_{LO} + \omega_{IF} \), again for integer \( n \), recognizing that to reconstruct time-domain waveforms one must account for the terms being omitted. Expressing the drain-source voltage and current responses at each of these frequencies as phasor sums denoted by primes:

\[ i'_{ds}(t) = \sum_{n=\infty}^{\infty} I_n e^{i\omega_n t}, \quad v'_{ds}(t) = \sum_{n=\infty}^{\infty} V_n e^{i\omega_n t} \]

allows them to be related by the Fourier series representation of the drain-source conductance:
\[ g_{ds}(t) = \sum_{n=-\infty}^{\infty} G_n e^{j\omega_n t}, \quad i'_{ds}(t) = g_{ds}(t) \cdot v'_{ds}(t) \]

to give the double sum:

\[ \sum_{k=-\infty}^{\infty} I_k e^{j\omega_n t} = \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} G_n V_m e^{j(\omega_n + \omega_m) t} \]

which can be viewed, finally, as a conversion matrix operation. Limiting the matrix to first-order mixing products, \( n \in \{-1,0,1\} \), gives a relation:

\[
\begin{bmatrix}
I'_{-1} \\
I'_0 \\
I'_1
\end{bmatrix} =
\begin{bmatrix}
G_0 & G_{-1} & G_2 \\
G_1 & G_0 & G_{-1} \\
G_2 & G_1 & G_0
\end{bmatrix}
\begin{bmatrix}
V'_{-1} \\
V_0 \\
V_1
\end{bmatrix}
\]

where the lower sideband frequency components are represented by conjugate coefficients\(^{66}\). In this manner, the response of the switch may be expressed in a compact and easily computed form. Note that for a linear circuit element, in which there is no interrelation between the responses at separate frequencies, the conductance matrix is diagonal.

Conductance matrices describe the linear part of a response and so may be used with linear circuit analysis techniques where matrix algebra is used to solve circuit quantities. To illustrate, assume some non-linear element with arbitrary 'conductance matrix' \( \bar{G}_x \) sits in parallel with a linear inductor of inductance \( L \) and a linear resistor of \( R \) Ohms and the response to first order is sought after, c.f. Figure 5.7.

\(^{66}\) Convention with phasors is to define complex coefficients for positive frequencies. For \( n < 0 \), \( \omega_n \) is negative and therefore must be recorded with a conjugate coefficient to redefine the matrix entries as coefficients of positive-frequency phasors \(^{65}\).
The 'impedance matrix' of the inductor is:

\[ \bar{sL} = \begin{bmatrix} -j\omega_{LO-IF}L & 0 & 0 \\ 0 & j\omega_{HF}L & 0 \\ 0 & 0 & j\omega_{LO+IF}L \end{bmatrix} \]

while the resistor has 'resistance matrix'

\[ \bar{R} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \]

where the currents flowing through the entire parallel network can be written in terms of the voltage across the network and an equivalent 'admittance matrix' at the frequencies of interest as:

\[ \bar{I} = \bar{Y}_{eq} \bar{V} = \left(\bar{R}^{-1} + \bar{sL}^{-1} + \bar{G}_x^{-1}\right)\bar{V} \]

### 5.2.2 Conductance Matrix of a pHEMT Switch

A preliminary to the analysis of the power mixer circuit is the proper derivation of the conversion matrix of the pHEMT switch used in the component amplifiers. Under the assumptions made in section 5.2.1, the goal is to find the matrix \( \bar{G} \) provided knowledge of the pHEMT model and the device size. The on-resistance of the device,
denoted \( R_{ON} \), is easily approximated from the triode region of the I/V curves of the device model by DC simulation. The switch conductance can then be approximated as in section 5.2.1 as moving from zero conductance (infinite resistance) to a conductance \( 1/R_{ON} \). Since the power in the mixing frequencies of interest results primarily from the DC and fundamental component of the time-varying conductance of the switch, it may be truncated for this analysis as \( g_{sq}(t) = g_0 + 2g_1 \cos(\omega_{LO}t) \) where the ideal and truncated waveform are shown for comparison in Figure 5.8.

![Figure 5.8](image)

**Figure 5.8** Time-varying conductance represented by ideal waveform \( g_{ds}(t) \) (red) and truncated representation \( g_{sq}(t) \) (blue).

To derive the conversion matrix coefficients of the switch, the Fourier series is expanded:

\[
g_{sq}(t) = g_0 + 2g_1 \cos(\omega_{LO}t) = \sum_{n=-1}^{1} G_n e^{jn\omega_{LO}t} \quad \Rightarrow \quad G_0 = g_0, \quad G_{-1} = G_1 = g_1
\]

\[
\Rightarrow \quad \bar{g}_{sq} = \begin{bmatrix} g_0 & g_1 & 0 \\ g_1 & g_0 & g_1 \\ 0 & g_1 & g_0 \end{bmatrix}
\]
With knowledge of the Fourier series describing the square wave of Figure 5.8 (note that its fundamental frequency component is weighted by $4/\pi$), the coefficients are fit with the on-resistance extracted from simulation to give the conversion matrix:

$$
\bar{g}_{sq} = \frac{1}{R_{ON}} \begin{bmatrix}
1/2 & 1/\pi & 0 \\
1/\pi & 1/2 & 1/\pi \\
0 & 1/\pi & 1/2
\end{bmatrix}
$$

Calculations with this conductance model were compared with harmonic balance simulations. The schematic shown in Figure 5.9 displays the simulated models. A pHEMT of on-resistance approximately 1.09 Ohms is switched by an ideal voltage source while being forced by voltage sources at the three mixing tones at its drain-source terminal. A second circuit model of an ideal switch with the same forcing was simulated concurrently, the drain current computation being performed independently in MATLAB for comparison. The results, shown below in Table 5.1, show good agreement between the idealized case and the computation using the conversion matrix above.

### Drain Current Response of pHEMT Treated As Ideal Switch (mA)

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Calculated</th>
<th>Switch Model</th>
<th>pHEMT Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\omega_{LO-IF}$</td>
<td>52.2</td>
<td>52.2</td>
<td>48.37</td>
</tr>
<tr>
<td>$\omega_{IF}$</td>
<td>66.4</td>
<td>66.5</td>
<td>64.57</td>
</tr>
<tr>
<td>$\omega_{LO+IF}$</td>
<td>38.4</td>
<td>38.3</td>
<td>33.64</td>
</tr>
</tbody>
</table>

Table 5.1 Comparison of calculated and simulated drain current amplitude for IF, image, and RF tones for verification of the conductance matrix of a single pHEMT switch.
The simulated gate drive of the pHEMT is a sinusoid at the LO frequency. The device therefore cannot transition instantly between the on and off states (however, the switch model, which agrees with the calculated expectation, does). The discrepancy between the behavior of the pHEMT and the ideal switch may be mitigated by modeling the pHEMT conductance as having only a DC and LO component as

\[ g_{\text{sine}}(t) = g_0 + 2g_1 \cos(\omega_{LO} t) \]

after deriving new Fourier coefficients \( g_0 \) and \( g_1 \).

These are seen to be \( g_0 = 1/(2R_{ON}) \) and \( g_1 = 1/(4R_{ON}) \), c.f. Figure 5.10, giving a
second conversion matrix:

$$\bar{g}_{\text{sine}} = \frac{1}{2 R_{\text{ON}}} \begin{bmatrix} 1 & 1/2 & 0 \\ 1/2 & 1 & 1/2 \\ 0 & 1/2 & 1 \end{bmatrix}$$

A comparison of computation of the current response to this conductance matrix with the harmonic balance results is shown below. The slightly underestimated current is likely due to error in the estimation of $R_{\text{ON}}$ from I/V curves:

**Drain Current Response of pHEMT Treated as 'Sinusoidal Conductance' (mA)**

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Calculated</th>
<th>pHEMT Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\omega_{\text{LO}-\text{IF}}$</td>
<td>44.9</td>
<td>48.37</td>
</tr>
<tr>
<td>$\omega_{\text{IF}}$</td>
<td>62</td>
<td>64.57</td>
</tr>
<tr>
<td>$\omega_{\text{LO}+\text{IF}}$</td>
<td>32.1</td>
<td>33.64</td>
</tr>
</tbody>
</table>

Table 5.2 Comparison of calculated and simulated current response to IF, image, and RF tones for verification of the conductance matrix of a single pHEMT switch.

Since the driving waveform in the power mixer is more closely modeled as a sinusoid than a square-wave, this second conductance matrix was used to analyze a modulated CMCD and the power mixer circuit in the succeeding sections. It should also be noted that in this step the LO and IF frequencies are kept low ($f_{\text{LO}}=1\,\text{MHz}$, $f_{\text{IF}}=1\,\text{kHz}$) and that the signal swing at the drain-source port kept the simulated device in the linear-resistance region with $V_{\text{DS}} < 0.34\,\text{V}$, well below the knee.

### 5.2.3 Analysis of a Modulated CMCD Amplifier

With the conversion matrix of a single pHEMT switch derived, increasingly complex circuit analyses can be performed. In this section, it is shown that a single

---

67 Using 1.05 Ohms gives good agreement, for instance.
CMCD used as a mixer does not show significant transparency – that is, the impedance seen looking into the IF port does not show high sensitivity to the RF load impedance. In fact, the IF driver sees roughly the series combination of the RF choke with the on-resistance of the switching devices.

A schematic of the transformer-coupled CMCD amplifier shown with quantities of interest is seen in Figure 5.11 with active devices represented by mixer equivalents. The complementary switches have conversion matrices $\bar{g}_1$ and $\bar{g}_2$:

$$
\bar{g}_1 = \frac{1}{2R_{ON}} \begin{bmatrix} 1 & 1/2 & 0 \\ 1/2 & 1 & 1/2 \\ 0 & 1/2 & 1 \end{bmatrix} \quad \frac{1}{2R_{ON}} \begin{bmatrix} 1 & -1/2 & 0 \\ -1/2 & 1 & -1/2 \\ 0 & -1/2 & 1 \end{bmatrix}
$$

Figure 5.11 Schematic of the drain-modulated, transformer-coupled CMCD amplifier with quantities of interest to conversion matrix analysis labeled.
It is assumed for simplicity that the two primary windings maintain perfect coupling to the secondary ( \( k=1 \) ), each with half the number of turns as the secondary winding.

The three-port description of the transformer may be written as a matrix equation:

\[
\begin{bmatrix}
V_1 \\
V_2 \\
V_3 
\end{bmatrix} =
\begin{bmatrix}
M_{11} & M_{12} & M_{13} \\
M_{21} & M_{22} & M_{23} \\
M_{31} & M_{32} & M_{33} 
\end{bmatrix}
\begin{bmatrix}
I_1 \\
I_2 \\
I_3 
\end{bmatrix}
\]

consisting of a matrix of 'conversion sub-matrices' \( \overline{M}_{ij} \), each diagonal in this example, which relate vector currents and voltages. The assumed 1:2 turns ratio from primaries to the secondary implies that \( L_3 = 4L_1 = 4L_2 \equiv 4L \), \( M_{13} = M_{23} = k\sqrt{4L_1 \cdot L_1} = 2L \), \( M_{12} = k\sqrt{L_1 \cdot L_1} = L \). Self inductances and reciprocity may also be accounted for to write:

\[
\begin{bmatrix}
V_1 \\
V_2 \\
0 
\end{bmatrix} =
\begin{bmatrix}
sL & sL & 2sL \\
sL & sL & 2sL \\
2sL & 2sL & Z_L + 4sL 
\end{bmatrix}
\begin{bmatrix}
T_1 \\
T_2 \\
T_3 
\end{bmatrix},
\overline{sL} =
\begin{bmatrix}
-j\omega_{LO-IF}L & 0 & 0 \\
0 & j\omega_{IF}L & 0 \\
0 & 0 & j\omega_{LO+IF}L 
\end{bmatrix}
\]

having applied Ohm’s law to the secondary loop and regrouped terms in the third row. It can be seen immediately that \( V_1 = V_2 \). Assuming the impedance of both the transformer winding and feed inductor are near zero at \( \omega_{IF} \) with \( \omega_{IF} \ll \omega_{LO} \), \( V_{2,0} = V_{1,0} = V_{3,0} = I_{3,0} = 0 \) and no magnetic flux couples to the secondary at the IF frequency. The IF and RF equivalent circuits may be analyzed in depth, as is provided in the first section of Appendix G to this thesis, to arrive at the following expression for the IF input impedance:
\[
Z_{IN,0} = \frac{R_{ON} + sL_1 \left(1 - \frac{4sL_1}{Z_{L,1} + 4sL_1}\right)}{1 + \frac{sL_1}{2R_{ON}} \left(1 - \frac{4sL_1}{Z_{L,1} + 4sL_1}\right) + \frac{1}{4} \left[ sL_1 \left(1 - \frac{4sL_1}{Z_{L,1} + 4sL_1}\right) - \frac{4sL_1^*}{Z_{L,1}^* + 4sL_1^*} \right] \left(1 - \frac{4sL_{-1}^*}{Z_{L,-1}^* + 4sL_{-1}^*}\right) + \frac{1}{4} \left[ R_{ON} + sL_{-1}^* \left(1 - \frac{4sL_{-1}^*}{Z_{L,-1}^* + 4sL_{-1}^*}\right) \right]
\]

(Eq. 5.2.3.1)

Evaluations of Equation 5.2.3.1 were compared to three simulations in which the load impedance of a transformer-coupled CMCD circuit was varied. First, the load resistance of a purely real load was swept. Second, series capacitance was added to a 50 Ohm load. Third, series inductance was added to a 50 Ohm load. All three simulations share drive levels and circuit parameters. In this manner the RF load impedance was moved around the complex plane while the impedance at the IF port, at low frequency, was observed. Figure 5.12 displays the three Agilent ADS schematics. In all three circuits, the transformer is modeled as three coupled coils with primary port inductances \(L\) of 10 nH (secondary winding inductance of 40 nH). Device \(R_{ON}\) is approximately 1.05 Ohms, center-tap feed inductor LS is 1.6 uH (0.001 Ohms-reactive at the IF frequency of 100 Hz – note that it is non-zero at the IF frequency and this reactance appears in series with the driver: it therefore must be subtracted from the harmonic balance results for comparison with Equation 5.2.3.1), and LO drives at 1 MHz.

---

68 This is equation G.1.9.
Figure 5.12 Schematics of simulated CMCD amplifier circuits for verification of conversion matrix analysis.

For trial one, in which the circuit of Figure 5.12(a) is solved for the set of load resistances $R_L = \{5, 10, 15, \ldots, 100\}$ Ohms, little variation in the IF input impedance of the mixer is seen\(^6\). For trial two, in which the circuit of Figure 5.12(b) is solved for a set

\(^6\) This is true of later simulations probing $R_L < R_{ON}$ (below 5 Ohms) performed after the transparency seen in section 5.2.4 was found with the image-reject mixer.
of capacitances which load the circuit at RF, again little variation is seen. For trial three, in which the circuit of Figure 5.12(c) is solved for a set of load inductances, little variation is seen. These results are tabulated in Figures 5.13 through 5.15.

<table>
<thead>
<tr>
<th>( R_L )</th>
<th>Simulated</th>
<th>MATLAB</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.000</td>
<td>1.072 + j0.001</td>
<td>1.053 + j3.049E-6</td>
</tr>
<tr>
<td>10.000</td>
<td>1.071 + j0.001</td>
<td>1.053 + j3.090E-6</td>
</tr>
<tr>
<td>15.000</td>
<td>1.071 + j0.001</td>
<td>1.052 + j3.101E-6</td>
</tr>
<tr>
<td>20.000</td>
<td>1.071 + j0.001</td>
<td>1.052 + j3.106E-6</td>
</tr>
<tr>
<td>25.000</td>
<td>1.071 + j0.001</td>
<td>1.052 + j3.109E-6</td>
</tr>
<tr>
<td>30.000</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.111E-6</td>
</tr>
<tr>
<td>35.000</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.112E-6</td>
</tr>
<tr>
<td>40.000</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.113E-6</td>
</tr>
<tr>
<td>45.000</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.114E-6</td>
</tr>
<tr>
<td>50.000</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.114E-6</td>
</tr>
<tr>
<td>55.000</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.115E-6</td>
</tr>
<tr>
<td>60.000</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.115E-6</td>
</tr>
<tr>
<td>65.000</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.115E-6</td>
</tr>
<tr>
<td>70.000</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.116E-6</td>
</tr>
<tr>
<td>75.000</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.116E-6</td>
</tr>
<tr>
<td>80.000</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.116E-6</td>
</tr>
<tr>
<td>85.000</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.116E-6</td>
</tr>
<tr>
<td>90.000</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.117E-6</td>
</tr>
<tr>
<td>95.000</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.117E-6</td>
</tr>
</tbody>
</table>

**Figure 5.13** Comparison of calculated and simulated IF input impedance of modulated CMCD vs. load resistance.

<table>
<thead>
<tr>
<th>( C_L )</th>
<th>Simulated</th>
<th>MATLAB</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.000E-9</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.114E-6</td>
</tr>
<tr>
<td>1.000E-8</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.114E-6</td>
</tr>
<tr>
<td>1.000E-7</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.114E-6</td>
</tr>
<tr>
<td>1.000E-6</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.114E-6</td>
</tr>
<tr>
<td>1.000E-5</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.115E-6</td>
</tr>
<tr>
<td>1.000E-4</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.120E-6</td>
</tr>
<tr>
<td>0.001</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.131E-6</td>
</tr>
</tbody>
</table>

**Figure 5.14** Comparison of calculated and simulated IF input impedance of modulated CMCD vs. additional series load capacitance.

<table>
<thead>
<tr>
<th>( L_L )</th>
<th>Simulated</th>
<th>MATLAB</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.000E-9</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.119E-6</td>
</tr>
<tr>
<td>1.000E-8</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.118E-6</td>
</tr>
<tr>
<td>1.000E-7</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.105E-6</td>
</tr>
<tr>
<td>1.000E-6</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.105E-6</td>
</tr>
<tr>
<td>1.000E-5</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.114E-6</td>
</tr>
<tr>
<td>1.000E-4</td>
<td>1.070 + j0.001</td>
<td>1.052 + j3.114E-6</td>
</tr>
</tbody>
</table>

**Figure 5.15** Comparison of calculated and simulated IF input impedance of modulated CMCD vs. additional series load inductance.

Noting that the on-resistance of the active device models used in simulation is roughly
1.05 Ohms (this is the value used in the MATLAB calculations) it is clear that the IF driver sees an input impedance nearly equal to the on-resistance of the active devices. To verify this assertion, a fourth simulation in which the transistor sizes – and therefore on-resistances – were varied was run with a static 50 Ohm load. Results confirming this intuition are seen in Figure 5.16. It is likely that the small discrepancy between simulated and calculated results is due to the simplified conversion matrix used to model the time-varying conductances: constant $R_{ON}$ is an approximation of the triode-region I/V characteristic of the pHEMTs, which may have non-linearities, and the swing of the gate drive may add unpredicted harmonic content to the simulation.

<table>
<thead>
<tr>
<th>R_ON</th>
<th>Simulated</th>
<th>MATLAB</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.253</td>
<td>$5.342 + 9.844E-4$</td>
<td>$5.233 + 3.14OE-6$</td>
</tr>
<tr>
<td>2.626</td>
<td>$2.672 + 9.973E-4$</td>
<td>$2.627 + 3.136E-6$</td>
</tr>
<tr>
<td>2.101</td>
<td>$2.138 + 9.999E-4$</td>
<td>$2.102 + 3.133E-6$</td>
</tr>
<tr>
<td>1.751</td>
<td>$1.782 + 0.001$</td>
<td>$1.752 + 3.130E-6$</td>
</tr>
<tr>
<td>1.501</td>
<td>$1.528 + 0.001$</td>
<td>$1.502 + 3.127E-6$</td>
</tr>
<tr>
<td>1.313</td>
<td>$1.337 + 0.001$</td>
<td>$1.315 + 3.123E-6$</td>
</tr>
<tr>
<td>1.167</td>
<td>$1.189 + 0.001$</td>
<td>$1.169 + 3.119E-6$</td>
</tr>
<tr>
<td>1.051</td>
<td>$1.070 + 0.001$</td>
<td>$1.053 + 3.114E-6$</td>
</tr>
</tbody>
</table>

**Figure 5.16** Comparison of calculated and simulated IF input impedance of modulated CMCD vs. switch on-resistance.

### 5.2.4 Analysis of the CMCD Power Mixer

The detailed schematic for the analysis of the image-reject CMCD mixer is presented in Figure 5.17. IF drivers encode information with $v_{I}(t)$, $\phi(t)$ using $v_{f} = v_{I}(t)\cos(\omega_{IF}t + \phi(t))$, $v_{q} = -v_{I}(t)\sin(\omega_{IF}t + \phi(t))$. The switches are operated by orthogonal LO drives $\pm \cos(\omega_{LO}t)$, $\pm \sin(\omega_{LO}t)$, giving the following conversion matrix descriptions of the pHEMT switches:
\[ \bar{g}_{1.2} = \frac{1}{2R_{ON}} \begin{bmatrix} 1 & \pm 0.5 & 0 \\ \pm 0.5 & 1 & \pm 0.5 \\ 0 & \pm 0.5 & 1 \end{bmatrix} \]

\[ \bar{g}_{3.4} = \frac{1}{2R_{ON}} \begin{bmatrix} 1 & \pm 0.5j & 0 \\ \mp 0.5j & 1 & \pm 0.5j \\ 0 & \mp 0.5j & 1 \end{bmatrix} \]

Figure 5.17 Schematic of the image-reject CMCD PA for conversion matrix analysis.

Secondary winding inductances are labeled such that the primary inductances may be tracked in the analysis by scaling by \( 1/n_i^2 \). The current vectors labeled for each transformer are indexed first by port number, as in the previous section, then location: transformer one is seen in the top left, two in the bottom left, three in the top right, and
four in the bottom right. Coupling coefficients $k_{ij}$ and turns ratios $n_{ij}$ between primaries and secondaries are left generalized, though the primary windings are assumed to be of equal number of turns and perfectly coupled within each transformer. For this analysis, which is detailed in section 2 of Appendix G, quantities are left expressed in terms of operations on matrices and vectors both for direct adaptation to MATLAB calculation and simplicity. The end result of the analysis of Appendix G.2 is a complicated expression for the input impedance seen by the first IF driver written in terms of the conversion matrices of the switching devices, properties of the transformers, and the load impedance, repeated in Equation 5.2.4.1 below:

$$Z_{IN,0} = \begin{pmatrix} \frac{1}{g_2^{-1} + g_2^{-1}\left(\frac{g_1^{-1}}{n_1} + 4\frac{sL_1}{n_1}\right)^{-1}} & (-\left(k_{11} + k_{12}\right)\frac{sL_1}{n_1} - \frac{1}{g_2^{-1} + 2\frac{sL_1}{n_1}}) \\ \frac{1}{g_2^{-1} + g_2^{-1}\left(\frac{g_1^{-1}}{n_1} + 4\frac{sL_1}{n_1}\right)^{-1}} & \frac{1}{g_2^{-1} + 2\frac{sL_1}{n_1}} \end{pmatrix} \begin{pmatrix} 1 \\ 0 \\ 0 \end{pmatrix}$$

(Eq. 5.2.4.1)

for $\bar{\alpha}$, $\bar{\beta}$ taken as:

$$\bar{\alpha} = j \left( k_{32} \frac{sL_3}{n_3} - k_{12} \frac{sL_4}{n_4} - (k_{31} + k_{32}) \frac{sL_3}{n_3} \left(\frac{1}{g_4^{-1} + g_3^{-1} + 4\frac{sL_3}{n_3}}\right)^{-1} \frac{1}{g_2^{-1} + 2\frac{sL_3}{n_3}} \right)$$

$$+ (k_{41} + k_{42}) \frac{sL_4}{n_4} \left(\frac{1}{g_4^{-1} + g_3^{-1} + 4\frac{sL_3}{n_3}}\right)^{-1} \frac{1}{g_2^{-1} + 2\frac{sL_4}{n_4}}$$

$$- \left( k_{12} \frac{sL_1}{n_1} - k_{22} \frac{sL_2}{n_2} - (k_{11} + k_{12}) \frac{sL_1}{n_1} \left(\frac{1}{g_1^{-1} + g_2^{-1} + 4\frac{sL_1}{n_1}}\right)^{-1} \frac{1}{g_2^{-1} + 2\frac{sL_1}{n_1}} \right)$$

$$+ (k_{21} + k_{22}) \frac{sL_2}{n_2} \left(\frac{1}{g_1^{-1} + g_2^{-1} + 4\frac{sL_1}{n_1}}\right)^{-1} \frac{1}{g_2^{-1} + 2\frac{sL_2}{n_2}}$$

170
\[
\beta = Z_L + sL_3 + sL_4 + sL_1 + sL_2 - \left( \frac{k_{31} + k_{32}}{n_3} \right)^2 \frac{sL_3}{\beta_4} + \frac{1}{\beta_3} + 4 \frac{sL_3}{n_3} - 2 sL_3
\]

\[
- \left( \frac{k_{41} + k_{42}}{n_4} \right)^2 \frac{sL_4}{\beta_4} + \frac{1}{\beta_3} + 4 \frac{sL_4}{n_4} - \left( \frac{k_{11} + k_{12}}{n_1} \right)^2 \frac{sL_1}{\beta_1} + \frac{1}{\beta_2} + 4 \frac{sL_1}{n_1} - 2 sL_1
\]

\[
- \left( \frac{k_{21} + k_{22}}{n_2} \right)^2 \frac{sL_2}{\beta_2} + \frac{1}{\beta_1} + 4 \frac{sL_2}{n_2} - \frac{1}{\beta_1}
\]

Equation 5.2.4.1 was studied and compared to harmonic balance results. The formula was first tested for sensitivity to a variable load impedance: it was found that if the load impedance is transformed down considerably with respect to 50 Ohms (an impedance scaling of 1/16 in these examples) before evaluating Eq. 5.2.4.1, transparency was observed. That is, the input impedance looking into each IF port (all four are equal) varies significantly for 'heavier' variable RF loads in the shared secondary. This is assumed to be due to the interaction of the I/Q half-circuits in a manner similar to the current-mixing in the work of Andrews and Molnar, noting that transparency was not seen in the single-mixer case of section 5.2.3 [64].

Calculated input impedance for several \( Z_L \) is shown in Figures 5.18 and 5.19, with the turns ratio shared by each of the four CMCD windings parameterized (one value per curve from the set \( n = \{0.25, 0.5, 0.75, 1, 1.25, 1.5, 1.75, 2\} \))\(^7\). The load impedance for the trial of Figure 5.18 is a parallel resistor \( R_L \) and capacitor \( C_L \) dictated by\(^7\):

\[
C_L = \frac{1}{(\omega_{LO} - \omega_{IF})} \sqrt{\frac{1}{50^2} - \frac{1}{R_L^2}}
\]

\(^7\) Circuit constants were \( R_{ON} = 1.05 \), \( f_{IF} = 100 \text{ Hz} \), \( f_{LO} = 10 \text{ MHz} \), \( L_1 = L_2 = L_3 = L_4 = 1.59 \mu \text{H} \).

\(^7\) The circuit is configured to transmit the lower side-band, the upper sideband is the image frequency.
for $R_L = 50, 51, \ldots, 200$ to keep a constant impedance magnitude of 50 Ohms per:

$$Z_L = \left( \frac{1}{R_L} + j(\omega_{LO} - \omega_{IF})C_L \right)^{-1}$$

with variable angle. For the trial of Figure 5.19, the load is a resistor $R_L$ in series with an inductor $L_L$ dictated by:

$$L_L = \frac{1}{(\omega_{LO} - \omega_{IF})} \sqrt{50^2 - R_L^2}$$

for $R_L = 1, 2, \ldots, 50$ Ohms to keep a constant impedance magnitude of 50 Ohms per $Z_L = R_L + j(\omega_{LO} - \omega_{IF})L_L$. It can be seen that rotating the load around the first quadrant at $\omega_{LO} - \omega_{IF}$ translates to elliptic arcs in the fourth quadrant at the IF port at $\omega_{IF}$, while rotating the load around the fourth quadrant shows elliptic arcs at the IF port in the first quadrant. Note also that a turns ratio of $n = 0.75$ for the transformers coupling the mixer-amplifiers shows widest variation in the imaginary part of the IF impedance – in addition, it shows almost purely imaginary variation. For every turns ratio $n$, the IF impedance corresponding to a real-valued RF load lands close to the real axis, with the IF impedance contours moving off that axis as the RF load becomes complex (and eventually almost entirely reactive).

The circuits of Figures 5.20 and 5.22 were simulated for comparison – note the transformer and components comprising the load(s). Similar to the calculation trials, the load impedance was varied while the IF input impedance at driver one was calculated from the harmonic balance results (again, all four IF drivers see the same input impedance).
Figure 5.18 Evaluation of IF impedance using Equation 5.2.4.1 with fourth-quadrant RF load impedance.
(a) RF load impedances taken as input to formula before 1/16 step-down, (b) evaluated IF input impedances.
Figure 5.19 Evaluation of IF impedance using Equation 5.2.4.1 with first-quadrant RF load impedance. (a) RF load impedances taken as input to formula before 1/16 step-down, (b) evaluated IF input impedances.
Simulated gate drive and drain modulation have identical levels to prior verification steps (0.7 V gate swing at -0.5 V DC bias, 0.17 V drain modulation with 0.17 V DC bias).

Devices were sized for $R_{ON} = 1.05$ Ohms with remaining circuit constants

$L_1 = L_2 = L_3 = L_4 = 1.59 \, \text{nH}$, $L_S = 1 \, \mu \text{H}$, $C_{-0} = 1/\left(\left(\omega_{LO} - \omega_{IF}\right)^2 L_1\right) = 0.16 \, \mu \text{F}$.

Results are shown with the simulated load impedance contours in Figures 5.21 and 5.23. Agreement within 5.5% of calculated predictions results. An example comparison is illustrated in Figure 5.24(a). If the devices are taken as having 1.1 Ohm on-resistance in calculation, the maximum error is 3.8%, with the tighter fit to simulation seen in Figure 5.24(b).

---

72 This capacitor is included to resonate the transformer winding inductance at the RF frequency. In *calculation* trials, a small $L_i$ shows no tuning. In *simulation*, a large $L_i$ disturbs the circuit operation. $C_{-0}$ reconciled the two issues.
Figure 5.21 Simulation results from the circuit of Figure 5.20 for comparison with the results of Figure 5.18. (a) Simulated load impedances, (b) simulated IF impedance results.
If the order of the harmonic balance simulation is increased from first-order, larger discrepancies between simulation and calculated predictions appear, as seen in simulated results of Figures 5.25 and 5.26, where the harmonic balance has been expanded to cover four additional harmonics of the LO and IF along with their first-order mixing tones: the locus of points comprising the IF impedances exists in a different part of the complex plane and spans a larger area. This implies that the first-order conversion matrices are an oversimplification of the response of a real circuit – it may be that significant power is mixing to higher harmonics and being converted down to IF.
Figure 5.23 Simulated results from the circuit of Figure 5.20 for comparison with the results of Figure 5.19. 
(a) Simulated load impedances, (b) simulated IF impedance results.
Figure 5.24 Comparison of simulated (o) and calculated (+) IF impedance for RF load rotation in the fourth quadrant. (a) Device on-resistance taken as 1.05 Ohms, (b) device on-resistance taken as 1.1 Ohms.
Figure 5.25 Capacitive load trial repeated with harmonic and mixing order 5 (black) shown with lower-order result (blue).

Figure 5.26 Inductive load trial repeated with harmonic and mixing order 5 (black) shown with lower-order result (blue).
Increasing the IF drive from 0.17 V peak with 0.17 V bias to 1.5 V peak and 1.5 V bias without changing the order shows similar disagreement, likely indicating the limits of small-signal conversion matrix analysis, c.f. Figures 5.27 and 5.28.

**Figure 5.27** Capacitive load trial repeated with IF swing increased to 1.5 V about a 1.5 V DC bias (black) shown with lower-order result (blue).

**Figure 5.28** Inductive load trial repeated with IF swing increased to 1.5 V about a 1.5 V DC bias (black) shown with lower-order result (blue).
5.3 Potential Application

Properties of interest in the application of the mixer include its efficiency, conversion gain, image-rejection ratio, and local oscillator feed-through. Section 5.3.1 discusses these topics, with section 5.3.2 devoted to work toward a practical realization of the mixer.

5.3.1 The Ideal Case

Simulations of the idealized circuit of Section 5.2 with a real 50 Ohm load were performed with efficiency taken as $P_{RF} / (P_{DC} + P_{IF})$, where $P_{RF}$ is the output power at the transmitted sideband, $P_{IF}$ is the total power delivered to the circuit from the four IF drivers, and $P_{DC}$ is the total DC power consumed by the circuit. As in the tuning simulations, the turns ratio of the four CMCD transformers was parameterized, seen in Figure 5.29, where the conversion gain is taken as $dB\left(P_{RF} / P_{IF}\right)$ alongside the efficiency versus IF power. Two-millimeter devices with $R_{ON}$ approximately 1.09 Ohms were used as before. From this result, $n = 0.25$ is seen as the optimum transformation ratio for conversion gain and efficiency, showing efficiencies above 40% and conversion loss of roughly 2 dB for a wide range of input powers. The simulated image frequency and LO content at the load were at least 80 dB below the RF.

73 The image-rejection ratio is taken as $P_{image}/P_{RF}$, while the 'carrier rejection ratio' – a measure of LO feed-through, is taken as $P_{LO}/P_{RF}$ where $P_{LO}$ is the power at the LO frequency flowing to the load. It should again be noted that the load is transformed down to $50/16 = 3.125$ Ohms.
Figure 5.29 (a) Efficiency and (b) conversion gain of mixer shown against drive level for several turns ratios $n$ with 2-mm pHEMTs.
The complexity of the switching waveforms across the pHEMTs, an example of
which is seen in Figure 5.30, is not well understood: it appears as though combining the
four amplifiers results in excessive power dissipation when the switches move from the
'on' to 'off' portions of their cycle\textsuperscript{74}. This occurs with traditional CMCDs having badly
timed gate drives or detuned harmonic terminations. In addition, some skew from the
expected half-sinusoid CMCD drain-source voltage is seen\textsuperscript{75}.

 Ideal Power Mixer: Switching Waveforms of 2-mm pHEMT at Peak IF Voltage (Top In-Phase Amplifier)

![Ideal Power Mixer: Switching Waveforms of 2-mm pHEMT at Peak IF Voltage (Top In-Phase Amplifier)](image)

**Figure 5.30** Drain-source voltage (red, –) and drain current (blue, ---) of 2-mm pHEMT in top in-phase amplifier at peak IF voltage.

The efficiency and conversion gain along the capacitive load contour from the
prior study with $n=0.25$ is shown in Figure 5.31, with the power levels concerned
shown in Figure 5.32. The result is intuitive: as the load becomes more reactive, less
power is delivered to it and less IF power flows into the circuit, while the DC power

\textsuperscript{74} 0.4 mA peak-to-peak flows into the gate of the device – the dissipation is not due to forward biasing the
gate-source junction.

\textsuperscript{75} The efficiency may be related to the IF frequency. A high IF frequency may skew the switching
waveforms from the traditional CMCD case more so than a low IF frequency, thereby wasting more
power.
absorbed remains fairly constant, thereby lowering the efficiency and conversion gain.

Figure 5.31 Efficiency and conversion gain of image-reject mixer along capacitive load contour used in tuning analysis.

Figure 5.32 Simulated RF output power with IF and DC absorbed power along capacitive load contour used in tuning analysis.

5.3.2 The Practical Case

Problems arise when considering how to implement the mixer for lab testing.
There are no 1:16 impedance-ratio, step-down transformers available off the shelf for an L-band design. Nonetheless, the mixer topology was studied for feasibility and transparency with the symmetric CMCD stage from the preliminary PA design of Chapter 2 (i.e., a resonant tank circuit is used for harmonic termination), with transmission line baluns replacing the four center-tapped transformers. Due to the need to maintain balance to the third harmonic, the same 1:1 balun as the PA design was used [52]. The PA sub-circuit and the mixer are seen in Figure 5.33 and Figure 5.34. Ideal transformers translate the single-ended port of the available balun model to two floating pins for the secondary connection. Note that the turns ratio of the ideal transformer coupling the load is 1:1. In the prior section the turns ratio was varied, while in this study it is left 1:1 and the load is swept for similar effect, as will be discussed.

The mixer was simulated with 9 dBm available LO drive to each PA, $f_{LO}=1\,GHz$, $f_{IF}=1\,MHz$, driver gate bias voltages -0.6 V, switching stage gate biases -0.65 V, 2-millimeter switches, 120-micron drivers, driver drain biases of 4.7 V, and switch drain biases of 2.35 V with 2.35 V IF swings\(^{76}\). Results of sweeping the real-valued load can be seen in Figure 5.35 – it is inefficient (under 10\%), though nearly half a Watt of power is delivered to the load at RF (upper sideband, or 'USB', here) and the image content is at least 35 dB down, with essentially no LO content leaking to the load (simulated hundreds of dB down, doubtful in reality).

\(^{76}\) These were the optimally efficient settings for the sub-circuit simulated independently without modulation with a 50 Ohm load (72.4% simulated drain efficiency).
Figure 5.33 PA sub-block used for study of practical mixer realization.
Figure 5.34: Symmetric CMCD-based mixer simulation.
Figure 5.35 Initial symmetric CMCD-based mixer simulation results.

It was conjectured that the large DC consumption of the circuit is due to disturbance of the harmonic terminations of each amplifier when the PAs are conglomerated. Interaction between the PAs must alter the impedance loading the transmission line balun of each PA, thereby altering the impedances presented to the switches. The top half-circuit PAs 'fight' the bottom half-circuit PAs at the LO frequency, keeping currents at $\omega_{LO}$ from flowing in the secondary – each balun is effectively terminated in an open circuit at $\omega_{LO}$ on the secondary side. Likewise, the left half-circuit of the mixer 'fights' the right half, open-circuiting the secondary-side balun loads at the image frequency (and lowering the impedance loading each balun at the RF
frequency, since all the PAs combine power there). It was thought that the balun must map these effective open-circuits to some intermediate or near-short terminations presented to the switches, increasing the DC loss. This is to say that the PAs see 'worse' terminations looking through a real balun as opposed to ideal transformers in the mixer circuit.

As an indirect test of this theory, quarter-wave transmission lines (at $\omega_{LO}$) of characteristic 25 Ohms were added to the PA sub-circuit between the transmission line balun and switches, c.f. Figure 5.36. In this way, any effective open-circuit on the load side of the transmission line balun which maps through the transformer to a low impedance is inverted to a near-open at the switch drains. Since the switches now see a near open load at the LO and image frequencies, closer the ideal-balan case, the power loss should decrease. With this change in place, repeating the simulation with variable load resistance shows increased efficiency, with the DC consumption of the entire circuit moving from over 4 W prior to the change to under 0.5 W, as seen in Figure 5.37.

![Figure 5.36 Modified output network of symmetric CMCD sub-block.](image)

77 Note that the 1:1 balun expects a 50 Ohm balanced termination, or 25 Ohm per leg.
To find possible transparency with the symmetric-CMCD based mixer, conditions similar to those of the work of Section 5.2 were simulated, results being shown in Figures 5.38 through 5.42. First, a variable resistive load with and without the quarter-wave line was simulated. Second, complex load contours around the right half-plane, with the quarter-wave line\textsuperscript{78}, using a variable load of 120 Ohm magnitude in the secondary loop were tested (120 Ohms showed the optimum efficiency in the study of Figure 5.37). Some transparency is seen, with the expected decreasing efficiency as the load becomes increasingly reactive. Here, efficiency is taken as $\frac{P_{RF}}{P_{DC} + P_{IF} + P_{LO}}$ accounting for the 18 dBm of LO drive required. Despite tuning possibilities, the peak efficiency and output power of 40%, 0.4 W, respectively, limit the possibilities for the circuit's application.

\textsuperscript{78} The case with no quarter-wave line showed little efficiency, even with a real load.
These findings support the following conclusions:

- Transparency is observed at the IF ports of the image-reject mixer based on a 1 GHz two-stage CMCD design using transmission line transformer baluns.

- Including impedance-inverting lines appears to help control the harmonic terminations of the constituent amplifiers and improve efficiency while affecting the transparency relationship between RF and IF impedances.

- A careful method of power combining might satisfy the terminating criteria of the PAs to create a highly efficient mixer that provides transparency, perhaps in the manner of a distributed active transformer [66]. Load mismatch correction or monitoring might follow.

Figure 5.38 IF input impedance of symmetric CMCD-based mixer with (right) and without impedance inverting lines (left) along resistive load contour of Figure 5.37.

Figure 5.39 IF input impedance of symmetric CMCD-based mixer with quarter wave lines (right) along capacitive load contour (left).
Figure 5.40 Performance of symmetric CMCD-based mixer with quarter wave lines along capacitive load contour of Figure 5.39.

Figure 5.41 IF input impedance of symmetric CMCD-based mixer with quarter wave lines (right) along inductive load contour (left).
Figure 5.42 Performance of symmetric CMCD-based mixer with quarter wave lines along inductive load contour of Figure 5.41.
The following are typical schematic representations of linear power amplifiers (classes A and B) and the classical class-C tuned amplifier shown with their accompanying waveforms, op. cit. Krauss, Bostian, and Raab [4]:

Class-A

Class-B
Class-C

Note: Conduction angle slightly under $\pi/2$ (distance $2\gamma$ radians) shown. Below, the class-C waveforms with saturation:
The following are simulated source-pull results with the class-D stage at gate-source bias voltages -0.5, -0.6, and -0.7 Volts for several drive power levels in the saturated, high-PAE region. PAE and output power contours are shown in 0.1% and 0.1 dB steps down from the maximum, respectively. The maximum PAE and drain efficiency are provided to the left of each plot, with markers showing the power-added efficiency and output power along example contours on the Smith chart.
PAE and Saturated Output Power Contours of Idealized Symmetric CMOS at Single Gate Bias Voltage and Available Driver Power

Available Power Per Driver (dBm):
- 12.000

Switch Gate Bias Voltage (V):
- 6.000

Maximum Output Power (dBm):
- 31.498

Maximum PAE:
- 0.745

Maximum Drain Efficiency:
- 0.777

PAE Step: 1%
Output Power Step: 1 dB

PAE and Saturated Output Power Contours of Idealized Symmetric CMOS at Single Gate Bias Voltage and Available Driver Power

Available Power Per Driver (dBm):
- 12.000

Switch Gate Bias Voltage (V):
- 6.000

Maximum Output Power (dBm):
- 32.024

Maximum PAE:
- 0.781

Maximum Drain Efficiency:
- 0.777

PAE Step: 1%
Output Power Step: 1 dB

PAE and Saturated Output Power Contours of Idealized Symmetric CMOS at Single Gate Bias Voltage and Available Driver Power

Available Power Per Driver (dBm):
- 12.000

Switch Gate Bias Voltage (V):
- 6.000

Maximum Output Power (dBm):
- 31.978

Maximum PAE:
- 0.742

Maximum Drain Efficiency:
- 0.755

PAE Step: 1%
Output Power Step: 1 dB

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APPENDIX C

SIMULATED SOURCE-STABILITY CIRCLES: CLASS-D STAGE

The following are source-stability circles calculated using the Parker-Skellern model of the 2-mm switching pHEMTs. Each set of either high-frequency or low-frequency stability circles is shown with an illustration of the bias point at which it was calculated.
APPENDIX D

SIMULATED LOAD-STABILITY CIRCLES: DRIVER STAGE

The following are load-stability circles of the 75-um pHEMTs used in the design calculated using the Parker-Skellern model. Each set is shown with an illustration of the bias point at which it was calculated.
APPENDIX E

SIMULATED SOURCE-STABILITY CIRCLES: DRIVER STAGE

The following are source-stability circles of the 75-um pHEMTs used in the design calculated using the Parker-Skellern model. Each set is shown with an illustration of the bias point at which it was calculated.
APPENDIX F

POST-MEASUREMENT SIMULATIONS

F.1 Comparison of Stabilized Simulations

The following figures compare the simulated performance of the PA design between the Parker-Skellern and Angelov models after back-fitting the changes made in the lab for stability:

Figure F.1.1 Comparison of simulated PA performance with the two large-signal models: (top) power gain, output power, and efficiencies, (bottom) DC power absorbed by each amplifier stage.
F.2 Comparison of Refined Simulations

The following figures compare the simulated performance of the PA design between the Parker-Skellern and Angelov models after stabilization and accounting for PCB features critical to the design:

![Graph showing comparison of simulated performance](image)

**Figure F.2.1** Power gain, output power, and efficiency of refined simulations.
**Figure F.2.2** DC power absorbed by each amplifier stage in refined simulations.

**Figure F.2.3** Finer view of power gain and output power in refined simulations.
F.3 A Short Variation Study

Being hand-wound, the baluns at the input and output of the PA are a large, and likely dominant, source of variation. Placing the first measured results somewhere in the space of outcomes resulting from this variation would help indicate that the refined simulations match reality within reason enough to be begin optimizing the input and output matching networks of the PA design. This was done as follows: there were 10 available S-parameter files for the balun. 100 pairs \((G_P, P_O)\) of peak power gain \(G_P\) and peak output power \(P_O\) can be tabulated using all possible input and output baluns, all else held equal in the simulations. The constellation of points \((G_P, P_O)\) in the plane represents a set of likely design outcomes. The measured results can be plotted along with them.

The constellation resulting from the Angelov-based simulation is seen in Figure F.3.1. The measurements on board one are within the constellation, while the data from board three have reasonable peak power gain but peak saturated output power roughly 7.1% lower than the lowest 'likely' result. Board four is left out of the comparison due to its low gain.

Another step of reassurance is extension of this approach to include mismatch at the output SMA connector, which is specified to peak VSWR of 1.2 at 1 GHz for the flexible RG-178 cable used. Repeating the simulations with VSWR boundary conditions of 1, 1.1 and 1.2 extends the space to the 300 points seen in Figure F.3.2. The results from both boards are within the constellation – therefore, the simulations were at least a decent starting point for tuning work.
Figure F.3.1 Measured results plotted with constellation of likely outcomes due to input/output balun variation.

Figure F.3.2 Measured results plotted with constellation of likely outcomes due to input/output balun variation and output SMA jack VSWR.

F.4 Comparison of Post-Tuning Simulation Results

The following figures compare the simulated performance of the PA design between the Parker-Skellern and Angelov models after stabilization, accounting for PCB features critical to the design, and the final step of tuning the input and output networks:
Figure F.4.1 Power gain, output power, and efficiency of refined simulations with input/output network alterations.

Figure F.4.2 DC power absorbed by each amplifier stage in refined simulations with input/output network alterations.
Figure F.4.3 Finer view of power gain and output power in refined simulations with input/output network alterations.

Figure F.4.4 Finer view of efficiency in refined simulations with input/output network alterations.
APPENDIX G

DETAILED CONVERSION MATRIX ANALYSES

G.1 Analysis of a Modulated CMCD Amplifier

This section details the analysis of a modulated current-mode class-D power amplifier by first repeating the introduction from the main text. Lengthy algebraic manipulations follow, showing finally an expression for the impedance seen by the IF driver.

A schematic of the transformer-coupled CMCD amplifier shown with quantities of interest is seen in Figure G.1.1 with active devices represented by mixer equivalents. The complementary switches have conversion matrices $\bar{g}_1$ and $\bar{g}_2$:

$$
\bar{g}_1 = \frac{1}{2R_{ON}} \begin{bmatrix} 1 & 1/2 & 0 \\ 1/2 & 1 & 1/2 \\ 0 & 1/2 & 1 \end{bmatrix}
$$

$$
\bar{g}_2 = \frac{1}{2R_{ON}} \begin{bmatrix} 1 & -1/2 & 0 \\ -1/2 & 1 & -1/2 \\ 0 & -1/2 & 1 \end{bmatrix}
$$

![Figure G.1.1 Schematic of the drain-modulated, transformer-coupled CMCD amplifier with quantities of interest to conversion matrix analysis labeled.](image)

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It is assumed for simplicity that the two primary windings maintain perfect coupling to the secondary \((k=1)\), each with half the number of turns as the secondary winding. The three-port description of the transformer may be written as a matrix equation:

\[
\begin{bmatrix}
V_1 \\
V_2 \\
V_3
\end{bmatrix} =
\begin{bmatrix}
M_{11} & M_{12} & M_{13} \\
M_{21} & M_{22} & M_{23} \\
M_{31} & M_{32} & M_{33}
\end{bmatrix}
\begin{bmatrix}
I_1 \\
I_2 \\
I_3
\end{bmatrix}
\]

consisting of a matrix of 'conversion sub-matrices' \(\overline{M}_{ij}\), each diagonal in this example, which relate vector currents and voltages. The assumed 1:2 turns ratio from primaries to the secondary implies that \(L_3 = 4L_1 = 4L_2 \equiv 4L\), \(M_{13} = M_{23} = k\sqrt{4L_1 \cdot L_1} = 2L\), \(M_{12} = k\sqrt{L_1 \cdot L_1} = L\). Self inductances and reciprocity may also be accounted for to write:

\[
\begin{bmatrix}
V_1 \\
V_2 \\
0
\end{bmatrix} =
\begin{bmatrix}
sL & sL & 2sL \\
sL & sL & 2sL \\
2sL & 2sL & \bar{Z}_L + 4\bar{s}L
\end{bmatrix}
\begin{bmatrix}
T_1 \\
T_2 \\
T_3
\end{bmatrix},
\bar{s}L =
\begin{bmatrix}
-j\omega_{LO-IF}L & 0 & 0 \\
0 & j\omega_{IF}L & 0 \\
0 & 0 & j\omega_{LO+IF}L
\end{bmatrix}
\]

having applied Ohm's law to the secondary loop and regrouped terms in the third row. It can be seen immediately that \(V_1 = V_2\). Assuming the impedance of the transformer winding and feed inductor are near zero at \(\omega_{IF}\) with \(\omega_{IF} \ll \omega_{LO}\), \(V_{2,0} = V_{1,0} = V_{3,0} = I_{3,0} = 0\) and no magnetic flux couples to the secondary at the IF frequency.
The IF equivalent circuit can be drawn as in Figure G.1.2 above, where phasor quantities at the IF frequency have been labeled. Expressing the IF components of $I_1$ and $I_2$ as a linear combination of node voltages from the mixer conversion matrix relations shows:

$$-I_{1,0} = \frac{1}{2} R_{ON} \left( \frac{1}{2} V_{g_1,0} + V_{g_1,1} \right)$$

$$I_{2,0} = \frac{1}{2} R_{ON} \left( -\frac{1}{2} V_{g_1,1} + V_{g_1,0} \right)$$

where it is clear from the IF equivalent circuit that $V_{g_1,0} = V_{g_2,0}$. These equations may be used to relate the currents flowing in the transformer primary to one another:

$$V_{g_1,0} = V_{g_2,0} = \begin{pmatrix} 1 \\ 0 \end{pmatrix} = \begin{pmatrix} g_2 \\ g_1 \end{pmatrix} \begin{pmatrix} 0 \\ 1 \end{pmatrix} = \begin{pmatrix} 1 \\ 0 \end{pmatrix} \Rightarrow I_{2,0} = 2 I_{1,1} + I_{1,0} + I_{1,1}$$

where it is clear from the equivalent circuit at the mixing products, seen below, that $I_{2,-1} = I_{1,-1}$ and $I_{2,1} = I_{1,1}$ by continuity of current. Therefore, $I_{1,0} = - I_{1,0} = I_{2,0} = I_{2,0} = I/2$. In addition, a virtual ground exists at the transformer center tap at the RF and image frequencies $\omega_{LO} \pm \omega_{IF}$ (referred to here as 'the sidebands'), as can be seen by observing the voltages across the mixers. For instance:
\[
V_{g_2,-1}^* = \left( g_2 I_2 \right) \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} = 2R_{ON} \left[ \frac{3}{2} I_{2,-1}^* + \frac{1}{2} I_{2,1} \right] \\
V_{g_1,-1}^* = \left( g_1 (-I_1) \right) \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} = 2R_{ON} \left[ -\frac{3}{2} I_{1,-1}^* - \frac{1}{2} I_{1,1} \right]
\]

which is true of the upper sideband as well. Further, considering that \( V_1 = V_2 \) is known, summing the voltages in the primary loop shows that
\[
V_{g_2,-1}^* + V_{2,-1}^* = V_{g_1,-1}^* - V_{1,-1}^* = 0 \Rightarrow -V_{g_2,-1}^* = V_{2,-1}^* = V_{g_1,-1}^* = V_{1,-1}^* \Rightarrow V_{x,-1} = 0 \text{ and } V_{x,1} = 0
\]
by the same reasoning. Therefore, the center tap is a virtual ground at the sideband frequencies. These results make intuitive sense: from circuit symmetry the swing about the center tap should be balanced.

\[\text{Figure G.1.3 Schematic of CMCD amplifier equivalent circuit at RF and image frequencies with quantities of interest to this conversion matrix analysis labeled.}\]

To derive the impedance \( Z_{IN,0} \) seen by the IF driver in terms of the load impedance, it is necessary to relate the response at node \( V_x \), which has been shown to consist of only an IF component, to the load impedance. First, the currents in the secondary may be related to the load and primary current from row three of the transformer relationships:
Using the conversion matrix of switch one with prior results, the primary currents at the sidebands can be related to the IF drive using the following relationship:

\[
\begin{bmatrix}
V_1 \\
V_2 \\
0
\end{bmatrix} = \begin{bmatrix}
\frac{sL}{2} & \frac{sL}{2} & \frac{2sL}{2} \\
\frac{sL}{2} & \frac{sL}{2} & \frac{2sL}{2} \\
\frac{2sL}{2} & \frac{2sL}{2} & Z_L + 4sL
\end{bmatrix} \begin{bmatrix}
I_1 \\
I_2 \\
I_3
\end{bmatrix} \rightarrow \begin{bmatrix}
\frac{-4sL^*_1 I_{2,-1}}{Z^*_{L,-1} + 4sL^*_1} \\
0 \\
\frac{-4sL_1 I_{2,1}}{Z^*_{L,1} + 4sL_1}
\end{bmatrix}
\]

With some algebra, all three rows may be used to relate the sideband currents in the primary to IF quantities and circuit constants as:

\[
\bar{g}_{i_1} V_{g_1} = -\bar{T}_1 = \begin{bmatrix}
-I^*_{1,-1} \\
\frac{I}{2} \\
-I^*_{1,1}
\end{bmatrix} = \frac{1}{2R_{ON}} \begin{bmatrix}
V^*_{g_{i,-1}} + \frac{1}{2} V_{g_{i,0}} \\
\frac{1}{2} V^*_{g_{i,-1}} + V_{g_{i,s}} + \frac{1}{2} V_{g_{i,1}} \\
\frac{1}{2} V_{g_{i,0}} + V_{g_{i,1}}
\end{bmatrix}
\]

(Eq. G.1.1)

and the voltage swing across the mixers at the sidebands can be related as:

\[
V^*_{g_{i,-1}} + V_{g_{i,s}} = 2R_{ON}I - 2V_{g_{i,0}}
\]

(Eq. G.1.3)

using the first and third row. Substituting what is known into either of the first two lines of the transformer description, the following is true:

\[
\begin{bmatrix}
\bar{V}_1 = \bar{V}_2 = sL[I_1 + I_2] + 2sL[I_3 = 2sL]
\end{bmatrix} = \begin{bmatrix}
I_{1,-1} \\
0 \\
I_{1,1}
\end{bmatrix} = \begin{bmatrix}
\frac{4sL^*_{L,-1} I^*_{1,-1}}{Z^*_{L,-1} + 4sL^*_1} \\
0 \\
\frac{4sL_1 I_{1,1}}{Z^*_{L,1} + 4sL_1}
\end{bmatrix} \begin{bmatrix}
V^*_{g_{i,-1}} \\
0 \\
V_{g_{i,1}}
\end{bmatrix}
\]

(Eq. G.1.4)

Rearranging Equation G.1.3 and equating it to the first row of Equation G.1.4 above (the row corresponding to the lower sideband) gives:
\[ 2R_{ON} I - 2V_{g_{i,0}} - V_{g_{i,1}} = 2sL^*_1 I^*_{1,-1} - \frac{8sL^*_1 2 I^*_{1,-1}}{Z^*_{L,-1} + 4sL^-_{1}} \]  

(Eq. G.1.5)

Rearranging Equation G.1.2 and equating to the upper sideband terms of Equation G.1.4 gives Equation G.1.6:

\[ V_{g_{i,1}} = 2sL_1 I_{1,1} (1 - \frac{4sL_1}{Z_{L,1} + 4sL_1}) = 2sL_1 (1 - \frac{4sL_1}{Z_{L,1} + 4sL_1}) (\frac{V_{g_{i,0}}}{2R_{ON}} - I - I^*_{1,-1}) \]  

(G.1.6)

Rearranging Equation G.1.5 for \( V_{g_{i,1}} \) and equating to Equation G.1.6 provides the lower sideband primary current in terms of circuit constants and the center-tap IF voltage:

\[ 2sL_1 (1 - \frac{4sL_1}{Z_{L,1} + 4sL_1}) (\frac{V_{g_{i,0}}}{2R_{ON}} - I - I^*_{1,-1}) = -2sL^*_1 I^*_{1,-1} (1 - \frac{4sL^*_1}{Z^*_{L,-1} + 4sL^-_{1}}) + 2R_{ON} I - 2V_{g_{i,0}} \]

Rearranging terms to express \( I^*_{1,-1} \) in terms of \( V_{g_{i,0}} \):

\[ I^*_{1,-1} = \frac{2R_{ON} I - 2V_{g_{i,0}} - 2sL_1 (1 - \frac{4sL_1}{Z_{L,1} + 4sL_1}) (\frac{V_{g_{i,0}}}{2R_{ON}} - I)}{2sL^*_1 (1 - \frac{4sL^*_1}{Z^*_{L,-1} + 4sL^-_{1}}) - 2sL_1 (1 - \frac{4sL_1}{Z_{L,1} + 4sL_1})} \]  

(Eq. G.1.7)

It remains to solve for \( Z_{IN,0} \equiv \frac{V_{x,0}}{I} = \frac{V_{g_{i,0}}}{I} \) by substituting for \( I^*_{1,-1} \). From line one of Equation G.1.1, the following is true: \( -I^*_{1,-1} = \frac{1}{2R_{ON}} \left[ V^*_{g_{i,-1}} + \frac{1}{2} V_{g_{i,0}} \right] \) where the lower sideband voltage \( V^*_{g_{i,-1}} \) is related to the lower sideband current \( I^*_{1,-1} \) by row one of Equation G.1.4 as:

\[ V^*_{g_{i,-1}} = 2sL^*_1 I^*_{1,-1} (1 - \frac{4sL^*_1}{Z^*_{L,-1} + 4sL^-_{1}}) \]

Therefore, the lower sideband current may be written in terms of the IF voltage across the mixers as:
\[ I_{1,-1}^* = \frac{1}{2} V_{g_{i,s}} - 2 R_{ON} - 2 sL_{-1}^* \left( 1 - \frac{4 sL_{-1}^*}{Z_{L,-1}^* + 4 sL_{-1}^*} \right) \]  

(Eq. G.1.8)

Finally, equating this to Equation G.1.7 above gives \( V_{g_{i,s}} = V_{x,0} \) in terms of circuit constants and the IF drive current \( I \):

\[ V_{x,0} = \frac{-2 \left[ 2 R_{ON} + 2 sL_{-1}^* \left( 1 - \frac{4 sL_{-1}^*}{Z_{L,-1}^* + 4 sL_{-1}^*} \right) \right] [2 R_{ON} - 2 V_{x,0} - 2 sL_1 \left( 1 - \frac{4 sL_1}{Z_{L,1}^* + 4 sL_1^*} \right) \left( \frac{V_{x,0}}{2 R_{ON}} - I \right)]}{2 sL_{-1}^* \left( 1 - \frac{4 sL_{-1}^*}{Z_{L,-1}^* + 4 sL_{-1}^*} \right) - 2 sL_1 \left( 1 - \frac{4 sL_1}{Z_{L,1}^* + 4 sL_1^*} \right)} \]

Where \( Z_{IN,0} = \frac{V_{x,0}}{I} \) may be found by dividing both sides by IF drive current \( I \) and rearranging terms:

\[ Z_{IN,0} = \frac{R_{ON} + sL_1 \left( 1 - \frac{4 sL_1}{Z_{L,1}^* + 4 sL_1^*} \right)}{1 + \frac{sL_1}{2 R_{ON} \left( 1 - \frac{4 sL_1}{Z_{L,1}^* + 4 sL_1^*} \right)} + \frac{1}{4} \left\{ sL_1 \left( 1 - \frac{4 sL_1}{Z_{L,1}^* + 4 sL_1^*} \right) - sL_{-1}^* \left( 1 - \frac{4 sL_{-1}^*}{Z_{L,-1}^* + 4 sL_{-1}^*} \right) \right\} \]

(Eq. G.1.9)

It is seen that the IF input impedance has some dependence on the load impedance at the upper and lower sidebands (\( Z_{L,1}, Z_{L,-1} \)). The sensitivity of \( Z_{IN,0} \) to these quantities is explored in section 5.2.3 of the main text.

G.2 Analysis of the CMCD Power Mixer

This section details the analysis of the CMCD power mixer by first repeating the introduction from the main text. Similar to the prior section of this appendix, lengthy manipulations follow, showing finally an expression for the impedance seen by an IF driver. The detailed schematic for the analysis of the image-reject CMCD mixer is presented in Figure G.2.1. IF drivers encode information with \( v_i(t), q(t) \) using \( v_i = v_i(t) \cos(\omega_{IF} t + q(t)), v_q = -v_i(t) \sin(\omega_{IF} t + q(t)) \). The switches are operated by
orthogonal LO drives $\pm \cos(\omega_{LO} t)$, $\pm \sin(\omega_{LO} t)$, giving the following conversion matrix descriptions of the pHEMT switches:

\[
\vec{g}_{1,2} = \frac{1}{2R_{ON}} \begin{bmatrix} 1 & \pm 0.5 & 0 \\ \pm 0.5 & 1 & \pm 0.5 \\ 0 & \pm 0.5 & 1 \end{bmatrix} \quad \vec{g}_{3,4} = \frac{1}{2R_{ON}} \begin{bmatrix} 1 & \pm 0.5j & 0 \\ \mp 0.5j & 1 & \pm 0.5j \\ 0 & \mp 0.5j & 1 \end{bmatrix}
\]

Figure G.2.1 Schematic of the image-reject CMCD PA used in this conversion matrix analysis.

Secondary winding inductances are labeled such that the primary inductances may be tracked in the analysis by scaling by $1/n_i^2$. The current vectors labeled for each transformer are indexed first by port number, as in the previous section, then location: transformer one is seen in the top left, two in the bottom left, three in the top right, and four in the bottom right. Coupling coefficients $k_{ij}$ and turns ratios $n_{ij}$ between
primaries and secondaries are left generalized, though the primary windings are assumed to be of equal number of turns and perfectly coupled within each transformer. For this analysis, quantities are left expressed in terms of operations on matrices and vectors both for direct adaptation to MATLAB calculation and simplicity. Though the circuit is more complex than that of Appendix G.1, the analysis is more easily understood since these quantities are not expressed in terms of phasor coefficients at each frequency.

To begin, the 3-port description of each transformer may be written as:

$$\begin{bmatrix} V_{1,1} \\ V_{2,1} \\ V_{3,1} \end{bmatrix} = \begin{bmatrix} sL_1/n_1 & sL_1/n_1 & k_{11}sL_1/n_1 \\ n_2/sL_1 & n_2/sL_1 & k_{12}sL_1/sL_1 \\ k_{11}sL_1/n_1 & k_{12}sL_1/n_1 & sL_1 \end{bmatrix} \begin{bmatrix} I_{1,1} \\ I_{2,1} \\ I_{3,1} \end{bmatrix}, \quad \begin{bmatrix} I_{3,1} \end{bmatrix} = \begin{bmatrix} T_{1,1} \\ T_{2,1} \\ T_{3,1} \end{bmatrix}$$

$$\begin{bmatrix} V_{1,2} \\ V_{2,2} \\ V_{3,2} \end{bmatrix} = \begin{bmatrix} sL_2/n_2 & sL_2/n_2 & k_{21}sL_2/n_2 \\ n_2/sL_2 & n_2/sL_2 & k_{22}sL_2/sL_2 \\ k_{21}sL_2/n_2 & k_{22}sL_2/n_2 & sL_2 \end{bmatrix} \begin{bmatrix} I_{1,2} \\ I_{2,2} \\ I_{3,2} \end{bmatrix}, \quad \begin{bmatrix} I_{3,2} \end{bmatrix} = \begin{bmatrix} T_{1,2} \\ T_{2,2} \\ T_{3,2} \end{bmatrix}$$

$$\begin{bmatrix} V_{1,3} \\ V_{2,3} \\ V_{3,3} \end{bmatrix} = \begin{bmatrix} sL_3/n_3 & sL_3/n_3 & k_{31}sL_3/n_3 \\ n_2/sL_3 & n_2/sL_3 & k_{32}sL_3/sL_3 \\ k_{31}sL_3/n_3 & k_{32}sL_3/n_3 & sL_3 \end{bmatrix} \begin{bmatrix} I_{1,3} \\ I_{2,3} \\ I_{3,3} \end{bmatrix}, \quad \begin{bmatrix} I_{3,3} \end{bmatrix} = \begin{bmatrix} -T_{1,3} \\ -T_{2,3} \\ T_{3,3} \end{bmatrix}$$
the forcing current $I_{f}$

Substituting out $V_{1,4}$, $V_{2,4}$, and $V_{3,4}$, noting the possible substitution of the load current into the third row of each equation. Making these substitutions and summing voltages around the secondary current loop allows writing:

$$
egin{bmatrix}
V_{1,4} \\
V_{2,4} \\
V_{3,4}
\end{bmatrix} =
\begin{bmatrix}
\frac{sL_4}{n_1} & \frac{sL_4}{n_1} & \frac{k_{41}sL_4}{n_4} \\
\frac{n_2}{sL_4} & \frac{n_2}{sL_4} & \frac{k_{42}sL_4}{n_4} \\
\frac{k_{41}sL_4}{n_4} & \frac{k_{42}sL_4}{n_4} & \frac{sL_4}{n_4}
\end{bmatrix}
\begin{bmatrix}
T_{1,4} \\
T_{2,4} \\
T_{3,4}
\end{bmatrix}
\quad , \quad T_{3,4} = - T_{L}
$$

(Eq. G.2.1)

which will be useful after substituting an as yet unknown relation of the primary currents to the IF forcing and load currents. Focusing first on the center-tap voltage $V_{x,1}$ of the first transformer and its primary-side currents:

$$V_{x,1} = \overline{g}_2^{-1} T_{2,1} + V_{2,1} = \overline{g}_1^{-1} ( - T_{1,1} ) - V_{1,1}, \quad T_{x,1} + T_{1,1} = T_{2,1}, \quad T_{x,1} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}
$$

may be combined with rows one and two ($V_{1,1}$ and $V_{2,1}$) of the transformer description of the first amplifier to write:

$$\overline{g}_2^{-1} [ T_{x,1} + T_{1,1} ] = - \overline{g}_1^{-1} T_{1,1} - ( V_{1,1} + V_{2,1} ) = - \overline{g}_1^{-1} T_{1,1} - 2 \frac{sL_1}{n_1} T_{1,1} - 2 \frac{sL_1}{n_1} T_{2,1} - ( k_{11} + k_{12} ) - \frac{sL_1}{n_1} T_{L}
$$

Substituting out $T_{2,1}$ gives a formula relating the current at port one of the transformer, the forcing current $T_{x,1}$, and the load current $T_{L}$:

$$[ \overline{g}_2^{-1} + \overline{g}_1^{-1} + 4 \frac{sL_1}{n_1} ] T_{1,1} + [ \overline{g}_2^{-1} + 2 \frac{sL_1}{n_1} ] T_{x,1} = - ( k_{11} + k_{12} ) \frac{sL_1}{n_1} T_{L}
$$

(Eq. G.2.2a)

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This approach can be taken to each of the four transformers in the power mixer to arrive at the remaining three relationships between primary current, IF, and load current:

\[
\begin{align*}
&\left[ g_1^{-1} + \frac{sL_2}{n_2^2} \right] T_{1,2} + \left[ g_1^{-1} + 2 \frac{sL_2}{n_2^2} \right] T_{x,2} = -(k_{21} + k_{22}) \frac{sL_2}{n_2} T_L \quad \text{(Eq. G.2.2b)} \\
&\left[ g_1^{-1} + \frac{sL_3}{n_3^2} \right] T_{1,3} + \left[ g_1^{-1} + 2 \frac{sL_3}{n_3^2} \right] T_{x,3} = \left( k_{31} + k_{32} \right) \frac{sL_3}{n_3} T_L \quad \text{(Eq. G.2.2c)} \\
&\left[ g_1^{-1} + \frac{sL_4}{n_4^2} \right] T_{1,4} + \left[ g_1^{-1} + 2 \frac{sL_4}{n_4^2} \right] T_{x,4} = \left( k_{41} + k_{42} \right) \frac{sL_4}{n_4} T_L \quad \text{(Eq. G.2.2d)}
\end{align*}
\]

where it should be reiterated that the currents flowing into the IF port are by design:

\[
\begin{align*}
T_{x,2} &= \begin{bmatrix} 0 \\ -I \end{bmatrix}, & T_{x,3} &= \begin{bmatrix} 0 \\ jI \end{bmatrix}, & T_{x,4} &= \begin{bmatrix} 0 \\ -jI \end{bmatrix}
\end{align*}
\]

Focusing once again on Equation G.2.1, the first dot product of the right-hand side may be expanded:

\[
\begin{bmatrix}
k_{31} \frac{sL_3}{n_3} \\
k_{32} \frac{sL_3}{n_3}
\end{bmatrix} \begin{bmatrix}
T_{1,3} \\
T_{x,3} + T_{1,3}
\end{bmatrix} = \left( k_{31} + k_{32} \right) \frac{sL_3}{n_3} T_{1,3} + k_{32} \frac{sL_3}{n_3} T_{x,3}
\]

and \( T_{1,3} \) may be substituted from Equation G.2.2c. Doing this for all four terms on the right hand side of Equation G.2.1 with each of Equations G.2.2 removes the primary-side currents from the equation altogether. Carefully applying these four substitutions to Equation G.2.1 and rearranging terms gives a lengthy formula for the load current in terms of the forcing current vectors and known quantities.
To write this formula in a more compact form, let $\tilde{\beta}$ be:

$$
\tilde{\beta} = Z + sL_3 + sL_4 + sL_1 + sL_2 - \left( \frac{k_{31} + k_{32}}{n_2} \right)^2 \frac{sL_3}{n_3} [\bar{g}^{-1} + \bar{g}^{-1} + 4 \frac{sL_3}{n_3}]^{-1} sL_3
$$

$$
- \left( \frac{k_{41} + k_{42}}{n_4} \right)^2 \frac{sL_4}{n_4} [\bar{g}^{-1} + \bar{g}^{-1} + 4 \frac{sL_4}{n_4}]^{-1} sL_4 - \left( \frac{k_{11} + k_{12}}{n_1} \right)^2 \frac{sL_1}{n_2} [\bar{g}^{-1} + \bar{g}^{-1} + 4 \frac{sL_1}{n_2}]^{-1} sL_1
$$

$$
- \left( \frac{k_{21} + k_{22}}{n_2} \right)^2 \frac{sL_2}{n_2} [\bar{g}^{-1} + \bar{g}^{-1} + 4 \frac{sL_2}{n_2}]^{-1} sL_2
$$

and substitute in the known current forcing vectors $T_{x,1}, T_{x,2}, T_{x,3}, T_{x,4}$, letting $\bar{\alpha}$ be:

$$
\bar{\alpha} = j \left( \frac{sL_3}{n_3} - k_{31} \frac{sL_4}{n_4} - \frac{k_{31} + k_{32}}{n_2} \right) \frac{sL_3}{n_3} [\bar{g}^{-1} + \bar{g}^{-1} + 4 \frac{sL_3}{n_3}]^{-1} \frac{sL_3}{n_3}
$$

$$
+ \left( \frac{k_{41} + k_{42}}{n_4} \right)^2 \frac{sL_4}{n_4} [\bar{g}^{-1} + \bar{g}^{-1} + 4 \frac{sL_4}{n_4}]^{-1} \frac{sL_4}{n_4}
$$

$$
- \left( \frac{k_{11} + k_{12}}{n_1} \right)^2 \frac{sL_1}{n_2} [\bar{g}^{-1} + \bar{g}^{-1} + 4 \frac{sL_1}{n_2}]^{-1} \frac{sL_1}{n_2}
$$

$$
+ \left( \frac{k_{21} + k_{22}}{n_2} \right)^2 \frac{sL_2}{n_2} [\bar{g}^{-1} + \bar{g}^{-1} + 4 \frac{sL_2}{n_2}]^{-1} \frac{sL_2}{n_2}
$$

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to write $T_L$ in a more compact form $T_L = \bar{\beta}^{-1}\bar{\alpha} \begin{bmatrix} 0 \\ I \\ 0 \end{bmatrix}$.

Since the formula for the load current is found, the equations relating the load current to the primary-side currents and forcing may be used to find primary side currents and other quantities as desired. For example:

$$T_{1,1} = \left[ g_1^{-1} + \frac{4sL_1}{n_1} \right]^{-1} \left[ -(k_{11} + k_{12}) \frac{sL_1}{n_1} \bar{\beta}^{-1}\bar{\alpha} - \left[ g_2^{-1} + \frac{2sL_1}{n_1} \right] \right] \begin{bmatrix} 0 \\ I \\ 0 \end{bmatrix}$$

Finally, to find the input impedance of driver one, the following must be evaluated:

$$Z_{IN,0} = \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix}$$

where $V_{x,1}$ can be written:

$$V_{x,1} = \bar{g}_2\left[ T_{x,1} + T_{1,1} \right] = \bar{g}_2^{-1} \left[ \bar{g}_2^{-1} + \bar{g}_1^{-1} + \frac{4sL_1}{n_1} \right]^{-1} \left[ -(k_{11} + k_{12}) \frac{sL_1}{n_1} \bar{\beta}^{-1}\bar{\alpha} - \left[ g_2^{-1} + \frac{2sL_1}{n_1} \right] \right] \begin{bmatrix} 0 \\ I \\ 0 \end{bmatrix}$$

to finish the analysis at the final goal:

$$Z_{IN,0} = \left( \bar{g}_2^{-1} + \bar{g}_2^{-1} \left[ \bar{g}_2^{-1} + \frac{4sL_1}{n_1} \right]^{-1} \left[ -(k_{11} + k_{12}) \frac{sL_1}{n_1} \bar{\beta}^{-1}\bar{\alpha} - \left[ g_2^{-1} + \frac{2sL_1}{n_1} \right] \right] \right) \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix}$$

(Eq. G.2.3)


[52] M/A-COM Technology Solutions , “Transformer 1:1 transmission line balun 5 to 3000 MHz ,” MABA-007871-CT1A40 datasheet


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