January 2008

Silicon Germanium (SiGe) Bipolor Dicke Radiometer Front End Receiver Chip

Randy L. Wolf
University of Massachusetts Amherst

Follow this and additional works at: https://scholarworks.umass.edu/theses

Retrieved from https://scholarworks.umass.edu/theses/76

This thesis is brought to you for free and open access by ScholarWorks@UMass Amherst. It has been accepted for inclusion in Masters Theses 1911 - February 2014 by an authorized administrator of ScholarWorks@UMass Amherst. For more information, please contact scholarworks@library.umass.edu.
SILICON GERMANIUM (SiGe) BIPOLAR DICKE RADIOMETER FRONT END RECEIVER CHIP

A Thesis Presented

by

RANDY L. WOLF

Submitted to the Graduate School of the University of Massachusetts Amherst in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL AND COMPUTER ENGINEERING

February 2008

Master of Science in Electrical and Computer Engineering
SILICON GERMANIUM (SiGe) BIPOLAR DICKE RADIOMETER FRONT END

RECEIVER CHIP

A Thesis Presented

by

RANDY L. WOLF

Approved as to content and style by:

______________________________
Robert W. Jackson, Chair

______________________________
K. Sigfrid Yngvesson, Member

______________________________
Omid Oliaei, Member

Christopher V. Hollot, Department Head
Department of Electrical and Computer Engineering
ACKNOWLEDGMENTS

I would like to thank my advisor Robert W. Jackson and the University of Massachusetts Faculty for providing the guidance and education allowing me to expand in this area of research. Also, I thank Steven C. Reising for taking the time to correspond with me on the system requirements for this project.

This project would not have been possible if not for the support of the IBM management team: John Ferrario, Jack Pekarik and upper management who provided encouragement and financial support. The following people at IBM: Robert Barry I thank many times for putting up with me to coming into his office to ponder things with him on his white board about how design kit items in layout relate to the ‘real’ world process: gate tie downs, substrate contacts, mim cap tie downs, transistor’s body contacts, etc… James Slinkman and Alan Botula who are part of the 8HP process engineering team provided valuable feedback on issues related to the fabrication of this design. I also thank James for expanding my understanding of the many process steps required for creating the actual end product, and for proof reading this material for accuracy. David Scagnelli and Keith Carrig I thank for Cadence support; Jay Rascoe and Susan Sweeney for providing test equipment needed for testing and lab support questions. Tahar Benalia at Cadence and Apandarshan Monga at IBM I thank for being there to answer my many questions about how the Assura extraction tool works, and design kit related questions to it. Last but not least for the IBM team I thank Ramana Malladi for answering questions related to the IBM transistors’ models allowing me to analyze the structure and adjust them according to the process data.
The amount of time I spent on this project in addition to my full time job required many hours of my attention away from my wife Jessica, family and friends, all of whom have been very understanding, especially my wife; her understanding and support at home made this project possible. I thank them all for their patience.
ABSTRACT

SILICON GERMANIUM (SiGe) BIPOLAR DICKE RADIOMETER FRONT END RECEIVER CHIP

FEBRUARY 2008

RANDY L. WOLF, B.S., DREXEL UNIVERSITY

M.S.E.C.E., UNIVERSITY OF MASSACHUSETTS AMHERST

Directed by: Professor Robert W. Jackson

Radiometers measures background radiation noise power of a target. The dominant quality factor of the radiometer is determined by how sensitive it is, so the lower the noise figure and the higher the gain, the more sensitive it is. It must also calibrate out any interfering noise such as sky background and system noise. Any change in gain of the radiometer receiver must also be taken into account. A Dicke radiometer compensates system gain and noise variation by switching between the target and a known noise source. To accomplish this, a single pole, double throw (SPDT) switch, switches between the receiving antenna and the noise source. The common terminal of the switch goes to the input of the low noise amplifier (LNA). This switch has a noise figure approximately equivalent to its loss and its noise is amplified by the LNA.

To eliminate the loss of the switch, this paper studies a new approach of combining the switch and the LNA to become a “switchable” LNA by designing a two-stage gain block with the first stage capable of switching between the two inputs. Because the first stage is amplifying, there is no signal loss.
This thesis investigates the new switching LNA and the design approach used in choosing the technology, the transistor size, biasing, extractions and matching. Two variations of the design were built using IBM’s SiGe 8HP 120nm process. The expected and measured results are compared. Results show a measured gain of 10dB and noise figure of 5dB at 19GHz. These results fall short of expectations for reasons explained in the thesis. The overall performance of this switching LNA is compared to the traditional methods. Performance criteria include gain, noise figure, isolation, matching and linearity vs. frequency and their stability vs. power and temperature variation. Power consumption, physical size and cost are also considered. The degree to which the two inputs track one another is discussed.
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>ACKNOWLEDGMENTS</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABSTRACT</td>
<td>v</td>
</tr>
<tr>
<td>LIST OF TABLES</td>
<td>ix</td>
</tr>
<tr>
<td>LIST OF FIGURES</td>
<td>xi</td>
</tr>
</tbody>
</table>

## CHAPTER

1. INTRODUCTION ................................................................................................................ 1
   1.1 Motivation .............................................................................................................. 1
   1.2 Thesis Outline ...................................................................................................... 2

2. FRONT END REQUIREMENTS FOR A DICKE RADIOMETER ........................................ 4
   2.1 Radiometer’s Function ......................................................................................... 4
   2.2 Dicke’s Solution ................................................................................................... 7
   2.3 Front End Requirements ...................................................................................... 10

3. SWITCHING LNA .......................................................................................................... 13
   3.1 Theory of Operation ............................................................................................ 13
   3.2 Technology .......................................................................................................... 16
   3.3 Matching ............................................................................................................. 32
   3.4 Layout ............................................................................................................... 38
   3.5 Post Layout Simulations ..................................................................................... 45

4. RESULTS ..................................................................................................................... 62
   4.1 LNA1 Measurements ............................................................................................ 62
   4.2 LNA2 Measurements ............................................................................................ 72

5. EXTRACTIONS AND MODELS REVISITED .............................................................. 79
   5.1 Beta and Design Kit Adjustment .......................................................................... 80
   5.2 Input Transmission Line Loss ............................................................................. 82
   5.3 LNA1 Extraction Revisited .................................................................................. 89
   5.4 LNA1 and LNA2 Extraction Comparison .............................................................. 96
6. CONCLUSIONS AND FUTURE WORK ................................................................. 99

6.1 Contributions .......................................................................................... 99

APPENDICES

A. ASSURA EXTRACTION ............................................................................. 106
B. BONDWIRE .............................................................................................. 117
C. LNA1 SIMULATION PLOTS ................................................................... 122
D. LNA2 SIMULATION PLOTS ................................................................... 141
E. TEST SETUP ......................................................................................... 144
F. MULTIBAND USE ............................................................................... 146

BIBLIOGRAPHY ........................................................................................... 150
# LIST OF TABLES

<table>
<thead>
<tr>
<th>Table</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1. The physical and electrical properties for the 5 metal layer process option. Source: IBM 8HP Design Guidelines.</td>
<td>18</td>
</tr>
<tr>
<td>3.2. Electrical Limits for the High Performance HBT</td>
<td>23</td>
</tr>
<tr>
<td>3.3. High-\textit{f}T (NPN) Device Parameter Comparison</td>
<td>25</td>
</tr>
<tr>
<td>3.4. DC Analysis for LNA1 and LNA2</td>
<td>47</td>
</tr>
<tr>
<td>3.5. LNA1 input ports comparison in relation to the output</td>
<td>58</td>
</tr>
<tr>
<td>3.6. LNA1 input ports comparison in relation to each other</td>
<td>59</td>
</tr>
<tr>
<td>3.7. LNA2 input ports comparison in relation to the output</td>
<td>59</td>
</tr>
<tr>
<td>3.8. LNA2 input ports comparison in relation to each other</td>
<td>59</td>
</tr>
<tr>
<td>4.1. LNA1 input ports measurement comparison in relation to the output</td>
<td>71</td>
</tr>
<tr>
<td>4.2. LNA1 input ports comparison in relation to each other</td>
<td>72</td>
</tr>
<tr>
<td>4.3. LNA1 Linearity, Switching and Temperature Variations</td>
<td>72</td>
</tr>
<tr>
<td>4.4. LNA2 input ports measurement comparison in relation to the output</td>
<td>78</td>
</tr>
<tr>
<td>4.5. LNA2 input ports comparison in relation to each other</td>
<td>78</td>
</tr>
<tr>
<td>4.6. LNA1 Linearity and Switching Times</td>
<td>78</td>
</tr>
<tr>
<td>5.1. Simulation versus measured data (Design Kit V1.0.3.1HP)</td>
<td>80</td>
</tr>
<tr>
<td>5.2. Simulation results for before and after beta adjustment for LNA1</td>
<td>80</td>
</tr>
<tr>
<td>5.3. Simulation result comparison between design kits including the beta adjustment for LNA1</td>
<td>81</td>
</tr>
<tr>
<td>5.4. Comparing ‘RLCK’ to ‘PEEC+LADDER’ extraction simulations for LNA2</td>
<td>84</td>
</tr>
<tr>
<td>5.5. Comparing ‘RLCK’, ‘PEEC+LADDER’ and post LC adjustments for LNA2</td>
<td>85</td>
</tr>
</tbody>
</table>
5.6. Comparing ‘RLCK’ and ‘PEEC+LADDER’ extraction simulations for LNA1 .................................................................89

5.7. Comparing ‘RLCK’, ‘PEEC+LADDER’ and post LC adjustments for LNA1 ........95

5.8. Comparing the value of matching components required for matching LNA1 and LNA2. ‘RLCK’ is the original values determined from the extraction using the standard ‘RLCK’ method. PEEC(1) is the values required to match measured data after extracting using the original design kit. PEEC(2) is the values required to match measured data after extracting using the latest design kit.................................................................98

6.1. Parameter list to compare LNA1 and LNA2 to the traditional Switch+LNA design approach. .................................................................100

A.1. Parasitic Components Extracted and Simulation Times vs. Extractions Method for LNA1. ........................................................................111

A.2. Parasitic Components Extracted and Simulation Times vs. Extraction Method for LNA2. .................................................................112
LIST OF FIGURES

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1.</td>
<td>The Dicke Radiometer</td>
<td>7</td>
</tr>
<tr>
<td>3.1.</td>
<td>Block Diagram of the “Switchable” Input LNA</td>
<td>13</td>
</tr>
<tr>
<td>3.2.</td>
<td>Detailed Switchable LNA</td>
<td>15</td>
</tr>
<tr>
<td>3.3.</td>
<td>CMOS Control Circuit</td>
<td>16</td>
</tr>
<tr>
<td>3.4.</td>
<td>Cross section showing the five metal layer option</td>
<td>18</td>
</tr>
<tr>
<td>3.5.</td>
<td>Inductor <em>rline</em></td>
<td>20</td>
</tr>
<tr>
<td>3.6.</td>
<td>Transmission line <em>singlewire</em></td>
<td>21</td>
</tr>
<tr>
<td>3.7.</td>
<td>Input Resistance (<em>r_b</em>) vs. Emitter Stripe Size and Collector Current</td>
<td>26</td>
</tr>
<tr>
<td>3.8.</td>
<td>Input Reactance (<em>x_b</em>) vs. Emitter Stripe Size and Collector Current</td>
<td>26</td>
</tr>
<tr>
<td>3.9.</td>
<td>Maximum 19GHz Signal Gain vs. Emitter Stripe Size and Collector Current</td>
<td>28</td>
</tr>
<tr>
<td>3.10.</td>
<td>Minimum 19GHz Noise Figure vs. Emitter Stripe Size and Collector Current</td>
<td>28</td>
</tr>
<tr>
<td>3.11.</td>
<td>Graph comparing <em>f_T</em> versus emitter stripe size and collector current</td>
<td>29</td>
</tr>
<tr>
<td>3.12.</td>
<td>Equivalent Noise Resistance at 19GHz with respect to emitter stripe size and <em>I_c</em></td>
<td>30</td>
</tr>
<tr>
<td>3.13.</td>
<td>Optimal Input Match at 19GHz with respect to emitter stripe size and <em>I_c</em></td>
<td>31</td>
</tr>
<tr>
<td>3.14.</td>
<td>Source Stability Circles for 10GHz to 40GHz</td>
<td>36</td>
</tr>
<tr>
<td>3.15.</td>
<td>Load Stability Circles for 10GHz to 40GHz. <em>Z_load</em> is the load that the LNA sees at its output</td>
<td>36</td>
</tr>
<tr>
<td>3.17.</td>
<td>Noise Figure Circles at 19GHz</td>
<td>37</td>
</tr>
<tr>
<td>Figure</td>
<td>Page</td>
<td></td>
</tr>
<tr>
<td>--------</td>
<td>------</td>
<td></td>
</tr>
<tr>
<td>3.18.</td>
<td>$</td>
<td>S21</td>
</tr>
<tr>
<td>3.19.</td>
<td>Matching Circuits</td>
<td>38</td>
</tr>
<tr>
<td>3.20.</td>
<td>LNA1 Layout</td>
<td>40</td>
</tr>
<tr>
<td>3.21.</td>
<td>Matching Circuit for Input 1</td>
<td>42</td>
</tr>
<tr>
<td>3.22.</td>
<td>LNA2 Layout</td>
<td>43</td>
</tr>
<tr>
<td>3.23.</td>
<td>Rollett’s Stability Factor for LNA1</td>
<td>48</td>
</tr>
<tr>
<td>3.24.</td>
<td>Stability Measure $</td>
<td>\Delta</td>
</tr>
<tr>
<td>3.25.</td>
<td>LNA1, Input#1 and Input#2 to Output gain including the 150pH wirebonds</td>
<td>50</td>
</tr>
<tr>
<td>3.26.</td>
<td>LNA1, Input#1 and Input#2 to Output gain without wirebonds</td>
<td>51</td>
</tr>
<tr>
<td>3.27.</td>
<td>LNA2, Input#1 and Input#2 to Output gain without wirebonds</td>
<td>51</td>
</tr>
<tr>
<td>3.28.</td>
<td>LNA1, Input#1 and Input#2 to Output noise figure including the 150pH wirebonds</td>
<td>52</td>
</tr>
<tr>
<td>3.29.</td>
<td>LNA1, Input#1 and Input#2 to Output Noise Figure without the wirebonds</td>
<td>53</td>
</tr>
<tr>
<td>3.30.</td>
<td>LNA2, Input#1 and Input#2 to Output Noise Figure without the wirebonds</td>
<td>53</td>
</tr>
<tr>
<td>3.31.</td>
<td>LNA1, Input#1 and Input#2 reflection coefficient magnitude response with wirebonds included</td>
<td>54</td>
</tr>
<tr>
<td>3.32.</td>
<td>LNA1, Output reflection coefficient magnitude for when Input#1 is on and when Input#2 is on. Both include the 150pH wirebonds</td>
<td>55</td>
</tr>
<tr>
<td>3.33.</td>
<td>LNA2, Input#1 and Input#2 reflection coefficient magnitude response</td>
<td>55</td>
</tr>
<tr>
<td>3.34.</td>
<td>LNA2, Output reflection coefficient magnitude for when Input#1 is on and when Input#2 is on</td>
<td>56</td>
</tr>
<tr>
<td>3.35.</td>
<td>LNA1, Control Voltage ‘VC’ vs. Collector Current of Q2 and Q3</td>
<td>60</td>
</tr>
<tr>
<td>3.36.</td>
<td>LNA1, Input#1 P1dB input compression point</td>
<td>61</td>
</tr>
<tr>
<td>4.1.</td>
<td>LNA1 gain comparison between Input#1 when active and Input#2 when active</td>
<td>64</td>
</tr>
</tbody>
</table>
4.2. LNA1 input return loss comparison between Input#1 and Input#2 in both states......................................................................................................................65

4.3. LNA1 output return loss comparison between Input#1 and Input#2 in both states......................................................................................................................65

4.4. LNA1 gain comparison from the output to the active input........................................66

4.5. LNA1 gain (isolation) between the output and active input to the inactive input ..........................................................................................................................67

4.6. Noise Figure for Input#2 of LNA1 at 20°C temperature........................................68

4.7. LNA1 Noise Figure versus Temperature........................................................................69

4.8. LNA1 Gain versus Temperature................................................................................70

4.9. LNA1 Input 1dB Compression Point for Input#1 and Input#2................................71

4.10. LNA2 gain comparison between the Input#1 when active and Input#2 when active .................................................................74

4.11. LNA2 input return loss comparison between Input#1 and Input#2 in both states......................................................................................................................74

4.12. LNA2 output return loss comparison between Input#1 and Input#2 in both states......................................................................................................................75

4.13. LNA2 gain comparison from the output to the active input ........................................75

4.14. LNA2 gain (isolation) between the output and active input to the inactive input ..........................................................................................................................76

4.15. Noise Figure for Input#1 of LNA2 at 20°C temperature........................................77

5.1. Smith chart plotting the two measured inputs and output match for LNA2. S(1,1), marked by M8, is the match for Input#1 when active. S(6,6), marked by M10, is the match for Input#2 when active. S(3,3) is the output match, marked by M11, when Input#1 is active and S(7,7) is the output match, marked by M12, when Input#2 is active....................................................................................87
5.2. LNA2 simulated input return loss for Input#1 and Input#2 when active. ‘S11 dB20_In1 On pееclad_sub’ is Input1 after extraction before matching adjustment. ‘S11 dB20_In2 On pееclad_sub’ is Input2 after extraction before matching adjustment. ‘S11 dB20_In1 On LC adjusted’ is Input1 after extraction and after matching adjustment. ‘S11 dB20_In2 On LC adjusted’ is Input2 after extraction and after matching adjustment. ........................................87

5.3. LNA2 simulated output return loss for Input#1 and Input#2 when active. ‘S22 dB20_In1 On pееclad_sub’ is Input1 after extraction before matching adjustment. ‘S22 dB20_In2 On pееclad_sub’ is Input2 after extraction before matching adjustment. ‘S22 dB20_In1 On LC adjusted’ is Input1 after extraction and after matching adjustment. ‘S22 dB20_In2 On LC adjusted’ is Input2 after extraction and after matching adjustment. .................88

5.4. LNA2 simulated gain for Input2. ‘S21 dB20_pееclad_sub’ is Input2 gain after extraction but before input and output matching adjustment. ‘S21 dB20_LC adj’ is Input2 gain after extraction and input and output matching adjustment. ........................................................................................................88

5.5. LNA1, Input1 magnified to show the degenerate and matching inductor ground return connections around the common emitter. ..........................................................................................91

5.6. Smith chart plotting the two measured inputs and output match for LNA1. S(1,1), marked by M8, is the match for Input#1 when active and S(5,5) is the match when Input#1 is inactive, S(6,6), marked by M9, is the match for Input#2 when active and S(2,2) is the match for Input#2 when inactive, S(3,3) is the output match when Input#1 is active and S(7,7) is the output match when Input#2 is active. ................................................................................................................92

5.7. LNA1, output magnified to show the matching inductor and MIM capacitors connecting the common base stage to the transmission line leading to the output pads (not shown). The transmission lines connect the two inputs common emitter stage has been removed. ........................................................................................................93

5.8. LNA1, Input2 simulations using the latest design kit and extraction deck. rfline uses the inductor model in the design kit. ‘flatten rfline’ had the inductors extracted before simulation. .................................................................................................95

A.1. LNA1 Layout Showing User Regions for PEEC extraction........................................110

A.2. LNA2 Layout Showing User Regions for PEEC extraction........................................112

A.3. LNA1 input matching inductor with five paralleled 1pF MIM capacitors to AC short the 19GHz to ground. .................................................................................................................................115
A.4. LNA1 output matching inductor five paralleled 1pF MIM capacitors to AC short the 19GHz to ground.............................................................................................................115

A.5. Simulation results comparing Assura extraction of matching inductor circuits to Agilent’s Momentum. S(1,1) is the Momentum result for the input matching inductor circuit shown in figure A.3. S(3,3) is the Spectre result from the Assura extraction for the input matching inductor circuit. S(2,2) is the Momentum result for the output matching inductor circuit shown in figure A.4. S(4,4) is the Spectre result from the Assura extraction for the output matching inductor circuit. ..................................................116

B.1. ‘BONDW_Shape’ parameters to be used by ‘BONDWn”.................................118

B.2. ‘BONDW_Usershape’ parameters to be used by ‘BONDWn”.............................118

B.3. Ground-Signal-Ground Wirebond Schematic Model.................................119

B.4. Smith Chart showing results from the Bondwire model in Figure B.3..............120

B.5. 125um pitch GSG layout of 550um long, 80um wide and 20um thick gold ribbon wire. ..........................................................................................................................121

B.6. Smith chart results for the GSG ribbon wire shown in Figure B.5. ....................121

C.1. LNA1 gain for Input 1 for all models with the wirebonds modeled..................123

C.2. LNA1 gain for Input#1 for all models without the wirebonds modeled ..........123

C.3. LNA1 noise figure for Input#1 for all models with the wirebonds modeled....123

C.4. LNA1 noise figure for Input#1 for all models without the wirebonds modeled.....................124

C.5. LNA1, Input#1 reflection coefficient magnitude response with wirebonds........124

C.6. LNA1, Output reflection coefficient response with wirebonds..........................125

C.7. LNA1, Gain (isolation) simulation from Output to Input#1 (on). ......................125

C.8. LNA1, Gain (isolation) simulation from Input#1 (on) to Input#2 (off)............126

C.9. LNA1, Gain (isolation) simulation from Input#2 (off) to Input#1 (on).............126

C.10. LNA1, Gain (isolation) simulation from Input#1 (off) to Output....................127
<table>
<thead>
<tr>
<th>Figure</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>C.11.  LNA1, Gain (isolation) from Output to Input#1 (off)</td>
<td>127</td>
</tr>
<tr>
<td>C.12.  LNA1 gain comparison between Input 1 and Input 2 with the wirebond modeled</td>
<td>128</td>
</tr>
<tr>
<td>C.13.  LNA1 gain comparison between Input 1 and Input 2 without the wirebond modeled</td>
<td>128</td>
</tr>
<tr>
<td>C.14.  LNA1 noise figure comparison between Input 1 and Input 2 with the wirebond modeled</td>
<td>129</td>
</tr>
<tr>
<td>C.15.  LNA1 noise figure comparison between Input 1 and Input 2 without the wirebond modeled</td>
<td>129</td>
</tr>
<tr>
<td>C.16.  LNA1 input match comparison between Input 1 and Input 2 with the wirebond modeled</td>
<td>130</td>
</tr>
<tr>
<td>C.17.  LNA1 input match comparison between Input 1 and Input 2 without the wirebond modeled</td>
<td>130</td>
</tr>
<tr>
<td>C.18.  LNA1 output match comparison between Input 1 and Input 2 with the wirebond modeled</td>
<td>131</td>
</tr>
<tr>
<td>C.19.  LNA1 output match comparison between Input 1 and Input 2 without the wirebond modeled</td>
<td>131</td>
</tr>
<tr>
<td>C.20.  LNA1 output to input gain (isolation) comparison between Input 1 and Input 2 with the wirebond modeled</td>
<td>132</td>
</tr>
<tr>
<td>C.21.  LNA1 output to input gain (isolation) comparison between Input 1 and Input 2 without the wirebond modeled</td>
<td>132</td>
</tr>
<tr>
<td>C.22.  LNA1 input match comparison between Input 1 and Input 2 when they are off with the wirebond modeled</td>
<td>133</td>
</tr>
<tr>
<td>C.23.  LNA1 input match comparison between Input 1 and Input 2 when off without the wirebond modeled</td>
<td>133</td>
</tr>
<tr>
<td>C.24.  LNA1 input to output gain (isolation) comparison between Input 1 and Input 2 when off with the wirebond modeled</td>
<td>134</td>
</tr>
<tr>
<td>C.25.  LNA1 input to output gain (isolation) comparison between Input 1 and Input 2 when off without the wirebond modeled</td>
<td>134</td>
</tr>
</tbody>
</table>
C.26. LNA1 output to input gain (isolation) comparison between Input 1 and Input 2 when off with the wirebond modeled.................................135
C.27. LNA1 output to input gain (isolation) comparison between Input 1 and Input 2 when off without the wirebond modeled..........................135
C.28. LNA1 input match for Input 1 without the wirebond modeled..................136
C.29. LNA1 output match when Input 1 is on without the wirebond modeled........136
C.30. LNA1 gain (isolation) from output to Input 1 when on without the wirebond modeled.......................................................................137
C.31. LNA1 gain (isolation) from Input 1, when on to Input 2, when off without the wirebond modeled..................................................137
C.32. LNA1 gain (isolation) from Input 2, when off to Input 1, when on without the wirebond modeled..................................................138
C.33. LNA1 gain (isolation) from Input 1, when off, to Output without the wirebond modeled.................................................................138
C.34. LNA1 gain (isolation) from Output to Input 1, when off, without the wirebond modeled.................................................................139
C.35. LNA1 1dB input compression point for Input 1 without the wirebond modeled..............................................................................139
C.36. LNA1 1dB input compression point for Input 2 with the wirebond modeled..............................................................................140
D.1. LNA2 input reflection comparing Input#1 and Input2 when they are off.........141
D.2. LNA2 gain (isolation) between the ‘off’ input to the ‘on’ input.....................142
D.3. LNA2 gain (isolation) between the ‘on’ input to the ‘off’ input.....................142
D.4. LNA2 input 1dB compression point for Input1............................................143
D.5. LNA2 input 1dB compression point for Input2............................................143
F.1. Gain (top) and noise figure (bottom) plots for Input1 tuned for 900MHz band..................................................................................146
<table>
<thead>
<tr>
<th>Figure</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>F.2.</td>
<td>147</td>
</tr>
<tr>
<td>Top plot is input return loss (S11) and output return loss (S22). Bottom plot is the gain from the output to the active input ‘Input1’ tuned for 900MHz band.</td>
<td></td>
</tr>
</tbody>
</table>

| F.3.   | 148  |
| Gain from active input to inactive input (S12), and gain from inactive input to active input (S21). Active input is tuned for 900MHz and inactive input is tuned for 1.8GHz. |

| F.4.   | 148  |
| Gain (top) and noise figure (bottom) plots for Input2 tuned for 1.8GHz band. |

| F.5.   | 149  |
| Top plot is input return loss (S11) and output return loss (S22). Bottom plot is the gain from the output to the active input ‘Input2’ tuned for 1.8GHz band. |

| F.6.   | 149  |
| Gain from active input to inactive input (S12), and gain from inactive input to active input (S21). Active input is tuned for 1.8GHz and inactive input is tuned for 900MHz. |
CHAPTER 1

INTRODUCTION

1.1 Motivation

The primary consideration in a receiver, of any kind, is how well it receives a signal without distorting it or masking it with noise. Maybe the most challenging application of a receiver is to apply it in a radiometer. Radiometers measure background radiation noise power of a target. This power is proportional to the target’s equivalent temperature as described by Planck’s black body radiation law. The quality of a radiometer is determined by the accuracy of its measurement of equivalent temperature in a given amount of time. A dominant factor is the noise figure of the system front end. The system must also calibrate out any system noise and gain variations. A Dicke radiometer addresses system gain and noise variation by comparing the target to a known power source; usually a calibrated noise source. To accomplish this, a single pole, double throw (SPDT) switch, switches between the receiving antenna and the calibrated source. The common terminal of the switch goes to the input of the low noise amplifier (LNA). This switch has a noise figure approximately equivalent to its loss and its noise is amplified by the LNA. But what if we could eliminate the switch loss and still keep the switching capability? If this can be done while preserving gain and keeping linearity, it would provide a lower noise figure overall and possibly less physical space and power consumption.

To accomplish this, my research studies a new approach of combining the switch and the LNA to become a “switchable” LNA by designing a two-stage gain block with
the second stage being fed by either one or the other of two amplifiers in the first stage. The choice of the first stage amplifier determines which input is passed through to the output. Since there is no separate RF switch, lossy switch noise is eliminated.

To demonstrate the effectiveness of this approach, this “switchable” LNA was designed for a specific radiometer application: measuring the brightness temperature of ocean sea foam in the K-band [10]. Research in measuring sea foam brightness temperature to determine wind speed and wind direction has been going on for the past decade. This interest stems from the National Science Foundation (NSF), the National Oceanic and Atmospheric Administration (NOAA), the Department of Defense, NASA and the Naval Research Laboratory (NRL).

Being successful in this application could also lead into the use of this approach in other applications such as receivers requiring switching between multi-bands; cellular bands: 900MHz and 1800MHz as an example. This would be accomplished by tuning each of the inputs to the desired frequency band for optimal noise figure and gain, and taking advantage of the broadband output match leading into a broadband mixer.

### 1.2 Thesis Outline

The outline of the thesis is as follows:

Chapter 2 discusses how the Dicke Radiometer works and the performance of current methods is briefly discussed. Performance criteria include gain, noise figure, isolation, matching and linearity vs. frequency: 18.7GHz to 19.3GHz, and their stability vs. power and temperature variation. Power consumption and physical size is also considered.
Chapter 3 discusses the idea behind the new switching LNA approach and compares the overall theoretical performance, based on the manufacture’s design kit models and extraction tools, of this design to the traditional methods at the bandwidth previously mentioned. Having two inputs require equal performance between them so their duality is discussed.

Chapter 4 presents a detailed analysis of the two measured device performances and compares this to their modeled data.

Chapter 5 analyzes the discrepancies between measurements in chapter 4 to the extractions in chapter 3 to determine what caused them. The chapter concludes with suggestions for improving correlation between simulations and measurements.

Chapter 6 summarizes the contribution of this work and compares the results of the switching cascode solution to the current method used in the radiometer. It concludes discussing the feasibility of using this technique in multi-band communication applications.
CHAPTER 2

FRONT END REQUIREMENTS FOR A DICKE RADIOMETER

2.1 Radiometer’s Function

A radiometer is a calibrated ‘passive’ radar device that measures background radiation noise power of a target. This power is proportional to the target’s equivalent temperature by Planck’s black body radiation law and the target size [1]. Planck’s black body radiation law for the single mode case is given by:

\[ Prad = \frac{hf}{(e^{hf/(kT)}-1)} \]  \hspace{1cm} (2.1)

where \( Prad \) is the power in Watts (W), \( h \) is Plank’s constant \((6.626\times10^{-34} \text{J} \cdot \text{s})\), \( f \) is frequency in Hertz, \( k \) is Boltzman’s constant \((1.38\times10^{-23} \text{J} / \text{K})\) and \( T \) is the temperature of the body measured in Kelvin (K). At microwave frequencies where \( hf < kT \), the denominator can be simplified to the Rayleigh-Jeans approximation:

\[ Prad = kT_b B \]  \hspace{1cm} (2.2)

Where \( T_b \) is the effective temperature of the body and \( B \) is the bandwidth of frequency in Hertz (Hz) [1][2].

The target size is determined by the distance traveled by the radiated power and the effective area of the radiometer’s antenna. In a non-bounded medium such as free space, the distance decreases the radiated power by \( 1/(4\pi r^2) \) because the power is radiated outward equally, expanding with distance \( r \). The term used to describe this is radiated power flux \( (S) \) with units \( \text{W/area} \), so that for an isotropic radiating source [1]:

\[ S = \frac{Prad}{(4\pi r^2)} \]  \hspace{1cm} (2.3)
Thus the power received from the radiometer antenna is:

\[ P_{\text{rec}} = A_{\text{eff}} S \quad (2.4) \]

Because the received power is Gaussian noise in nature given by equation 2.2, the received power can also be given as:

\[ P_{\text{rec}} = kT_A B \quad (2.5) \]

where \( T_A \) is the equivalent antenna temperature. Combining equations 2.4 and 2.5 and simplifying gives:

\[ T_A = T_b * A_{\text{eff}} / (4\pi r^2) \quad (2.6) \]

Equation 2.6 shows that the antenna temperature is directly proportional to the target’s equivalent temperature also known as *brightness temperature* [1][3].

Integrating the detected signal for time \( \tau \), produces \( B\tau \) independent measurements of filtered noise. Having more samples provides a better the estimate of the standard deviation \( \sigma \), and so the better estimate of the temperature \( T_A \). The equated relationship of this uncertainty is:

\[ \Delta T = T_A / \sqrt{(B\tau)} \quad (2.7) \]

The bandwidths being predominantly determined by passive filters can be considered well behaved. The integration time is also well controlled.

Unfortunately other noise sources besides \( T_b \) are added to \( T_A \) such as noise due to the physical temperature of the antenna itself (\( T_p \)) and the physical temperature of any transmission line (\( T_o \)) between the antenna and the receiver, coupled with any noise added by the receiver’s equivalent noise temperature (\( T_n \)) [1][3][7]. Taking all of these noise sources into account for the total noise power measured by the radiometer (\( P_s \)) can be shown as:
\[ P_s = k(T_a + T_n)B \]  \hspace{1cm} (2.8)

where \( T_n \) is the receiver’s equivalent noise temperature and \( T_a \) takes into account the additional noise sources from the antenna to the receiver first stage, usually a switch or coupler:

\[ T_a = T_A e^{-2\alpha l} + \left( \frac{1}{e_a} - 1 \right) T_p e^{-2\alpha l} + T_o (1 - e^{-2\alpha l}) \]  \hspace{1cm} (2.9)

where

- \( T_A \) is given by eq. (2.6)
- \( \alpha \) = attenuation coefficient of transmission line (Np/m)
- \( l \) = length of transmission line (m)
- \( e_a \) = thermal efficiency of antenna (dimensionless)
- \( T_p \) = physical temperature of the antenna (K)
- \( T_o \) = physical temperature of the transmission line (K)

Equation 2.9 shows that the detected signal is the sum of all these noise sources and the problem is to distinguish the target noise signal from the interfering noise. The radiometer function is to carry out this task [1]. The added temperatures are relatively stable except for \( T_a \). \( T_n \) and any gain variation of the receiver must also be taken into account because this will affect the uncertainty of equation 2.7.

How stable the gain must be depends on the total temperature \( (T_a + T_n) \) and the required maximum uncertainty temperature \( \Delta T \). An example is a typical total temperature of 50K and a resolution of \( \Delta T = 5\text{mK} \) is required. This would require that the gain must vary less than \( 10\log_{10}(50.005/50) = 0.004\text{dB} \). This is very difficult to maintain when considering that a typical receiver having 100MHz bandwidth would
receive a total power of 6.9E^-19 Watts. Most detectors require an order of 1 – 10mW, so a total gain of 110dB would be needed and still maintain less than 0.004dB of gain variation during the integration time. A solution to this problem is given next.

2.2 Dicke’s Solution

In 1946 Robert Dicke proposed a solution to greatly reduce the stability problem of gain and varying system noise. The solution was to switch between a reference noise source and unknown noise from the antenna. A diagram of this system is shown in Figure 2.1

\begin{center}
\includegraphics[width=1\textwidth]{Figure_0.1.png}
\end{center}

**Figure 0.1** : The Dicke Radiometer

The radiometer is switched between the antenna and a reference temperature at a frequency \(F_s\). The output of the square law device is multiplied by a +1 or -1 at the same frequency to keep it in sync with the switch. The effect of this is the integrator sees a voltage of \(+c(T_a + T_n)G\) for one half period of \(F_s\) and \(-c(T_{\text{ref}} + T_n)G\) for the second half. \(F_s\) must be fast enough so that \(T_a, T_n\) and \(G\) can be considered a constant, and that the period is much less than the integration time \(\tau\). The result of the output voltage from the integrator is:

\[
V_{out} = c(T_a + T_n)G - c(T_{\text{ref}} + T_n)G = c(T_a - T_{\text{ref}})G \tag{2.10}
\]

Equation 2.10 shows that the Dicke radiometer removes the system noise \(T_n\) and the difference between \(T_a\) and \(T_{\text{ref}}\) is multiplied by the gain. Choosing \(T_{\text{ref}}\) to be similar to \(T_a\)
will reduce the weight of the gain compared to the traditional method of multiplying the gain to the sum of $T_a$ and a large $T_n$ [7]. If another known noise source is coupled to $T_a$ and adjusted so that $T_a = T_{ref}$, then the output of the integrator will be zero. This method is known as the Noise Injected Radiometer (NIR) [7].

Regardless if using the Dicke radiometer by itself or in a NIR, the penalty of adding a switch for improved stability is that the integration time for $T_a$ is reduced by half, because the integration time is split equally between these two states. Applying this to equation 2.7 shows that the uncertainty of the measurement of $T_a$, and $T_{ref}$ is respectively:

$$\Delta T_1 = \frac{(T_a + T_n)}{\sqrt{(B\tau/2)}} \quad (2.11)$$

$$\Delta T_2 = \frac{(T_{ref} + T_n)}{\sqrt{(B\tau/2)}} \quad (2.12)$$

These two equations are statistically independent so the uncertainty from each integration time is:

$$\Delta T = \sqrt{[\Delta T_1]^2 + \Delta T_2^2]} \quad (2.13)$$

Since $T_{ref}$ is chosen to be close to $T_a$, $T_{ref}$ can be replaced by $T_a$ simplifying equation 2.14 to:

$$\Delta T = \frac{2(T_a + T_n)}{\sqrt{B\tau}} \quad (2.14)$$

Equation 2.14 shows that the Dicke method to improve accuracy doubles the uncertainty.

*Selectivity* of a receiver is important, which is the ability to reject unwanted frequencies from the wanted frequency [8]. Filters function to improve this criterion, but also the antennas used are often highly directive and setup in an environment to avoid interfering tones from coupling into the receiver. However, the most important criteria of a radiometer is it’s *sensitivity*, which is the ability to detect weak signal from
interfering noise such as those mentioned previously. Sensitivity is determined by the minimum signal-to-noise ratio (SNR) needed to detect the signal from the noise and Equation 2.7 determines, in part, the sensitivity of the radiometer. This can be shown by setting the SNR to 1 as the minimum detection, which sets the power received equal to the noise power of the receiver \( P_{\text{rec}} = P_n \) or:

\[
kT_aB = kT_nB \quad (2.15)
\]

\( k \) and \( B \) cancels and \( T_a \) of equation 2.9 can be approximated as \( T_A \) if care is taken to keep insertion loss due to the transmission to a minimal. Using equation 2.6 to substitute for \( T_A \) shows at SNR =1:

\[
A_{\text{eff}} \frac{T_b}{(2\pi r^2)} = T_n \quad (2.16)
\]

Using equation 2.7 and rearranging it shows:

\[
A_{\text{eff}} \Delta T \sqrt{(B\tau)/(2\pi r^2)} = T_n
\]

or isolating \( \Delta T \):

\[
\Delta T = \frac{T_n(2\pi r^2)}{(A_{\text{eff}}\sqrt{(B\tau)})} \quad (2.17)
\]

Multiplying both sides by Boltzman’s constant to convert uncertainty of temperature to power sensitivity leads to:

\[
\Delta P = kT_n(2\pi r^2)/(A_{\text{eff}}\sqrt{(B\tau)}) \quad (2.18)
\]

Equation 2.18 shows that the sensitivity of the radiometer is decreased with the increase in \( T_n \) and distance, but improved with increase of the effective antenna area, bandwidth or integration time.
2.3 Front End Requirements

A Current System

The previous sections focused on parameters that must be considered when designing the front end of a radiometer receiver. Those parameters will now be taken into account to evaluate a system currently in place to measure sea foam brightness temperature in the K-band. The frequency of interest in this band is 18.7GHz to 19.3GHz providing a bandwidth of 600MHz. The current system uses a GaAs PIN diode SPDT (HMC347, Hittite) and a three stage GaAs LNA (CHA2193, UMS) [9]. The performance of these components at 19GHz is 1.9dB loss and 1.9dB noise figure (NF) for the SPDT, and 17.4dB gain and 2.25dB NF for the LNA. This gives the total front end performance of 15.5 dB gain and a 4.15dB NF.

The return loss for the switch is better than 15dB, but the LNA dominates with an input and output return of about 9.5dB. It was sought to better this by 2.5dB. The limiting linearity factor between the LNA and switch is the LNA, which has an input 1dB compression point (Pin1dB) of -9.4dBm. This however is not a strict requirement because the linearity of the overall system will be limited by the gain stages that follow beyond the LNA. The LNA consumes 60mA to 100mA biased at a drain voltage of 3.5VDC and with a negative gate voltage supply of approximately -1VDC. The gain flatness of the LNA for this bandwidth is +/- .25dB. The LNA chip dimensions are 2.07 x 1.03 x .10 mm. The GaAs PIN diodes operate between 0 and -5VDC with less than 50uA of current draw. It has an insertion loss of 1.9dB at 19GHz. The isolation between inputs of the switch is 43dB. The isolation between the off input and common port is 35dB. Switching time is < 6ns. The switch chip dimensions are 0.8 x 1.3 x .10 mm. The
Gain and noise figure variations vs. temperature and supply power are not provided for either part but field experiments has proven that the combination allows a radiometer sensitivity of 0.2K for 1s integration time. However, the next generation radiometer is expected to have a sensitivity of 0.1K for 100ms integration time.

_Target Specifications_

It was shown in this chapter that the Dicke method eliminates errors due to gain variation during the integration time, but the gain still must stay stable within the switching times. Given a $T_A \approx 300K$ and $\Delta T = 0.1K$, indicate that the gain stability must be $10\log_{10}(300.1K/300K) = 0.001$dB during the switching frequency $1/F_s$, which is typically $1/100^{th}$ of the integration time = 1ms. The temperature 300K is used as worse case as sea foam brightness temperature is typically less than 220K [10]. The targeted gain difference between the two ports is 0dB, but differences can be calibrated out like that done for the current system. It is more important that the two ports’ gain is within 0.001dB of each other after each switching period at a given temperature. Putting this data together along with the current system specifications sets the requirements for this project:

1. Frequency of operation: 18.7Ghz – 19.3GHz
2. Total Noise Figure < 4.15 dB at 19GHz.
3. Gain => 15dB
4. Gain Flatness <= 0.5 dB in 600MHz
5. Gain change of less than 0.01dB/°C centered at 22°C for both ports.
6. Gain fluctuations for both ports less than 0.001dB at 22°C using DC supply having .003% RMS noise.
7. Input 1dB compression point (IP1dB) =>-40dBm
8. Isolation between the “off” input port to the output and “on” input port => 35dB
9. Switching times (10/90% RF) < 1% of 1ms/2 = 5us
10. Power consumption < 60mA@3.5VDC
11. IC size less than total size taken by switch and LNA, extra board space for wire-bonding the two together not included. Current method die area is 3.37mm x 1.83mm = 6.17mm^2.

12. As few connections and voltage controls as possible.

13. Best port match possible with reflection not to be worse than 12dB.
CHAPTER 3

SWITCHING LNA

In this chapter I first outline the basic circuit operating principle. Then the relevant IBM passive and active technology is reviewed. A section on matching circuits is followed by a section on a layout description. Lastly, detailed simulation results are discussed.

3.1 Theory of Operation

The previous chapter showed that the majority of SNR degradation in the current radiometer front end is due to the switch having close to 2dB insertion loss. To eliminate the loss of this switch, a new circuit was developed to combine the switch and LNA to become a “switchable” LNA by designing a two stage gain block with the first stage capable of switching between the two inputs. Figure 3.1 shows a simplified block diagram of the concept.

![Figure 0.1: Block Diagram of the “Switchable” Input LNA](image)

This will reduce the system noise figure if the “switchable” LNA noise figure is kept lower than the combined switch and LNA noise figure. Either a cascade or a cascode topology could be used to implement this design, but the cascode topology was chosen.
because it provides improved bandwidth by decreasing the Miller capacitance, it was easier to modify for this implementation, and it provides a large output resistance. The latter allows the possibility of broadband-matching for possible use in other lower frequency applications.

The technology available for the RF gain stages offered either SiGe bipolar transistors or CMOS field effect transistors. The SiGe bipolar transistor was chosen because it provides lower noise properties and higher gain at 19GHz compared to CMOS at the time of this study. CMOS is useful for turning on and off the input stages of the amplifier and consumes less power. Several iterations were done with a three port single ended topology until the design shown in Figure 3.2 was chosen. The three ports are INPUT #1, INPUT #2 and OUTPUT with each input having matched signal paths. The cascode transistors are Q1 and either Q2 or Q3.

The design works by supplying 2.25VDC (located at the top of the figure) to the bipolar transistors. Current flows from the top half down to either the left half or the right half depending on the voltage biasing the NMOS gates Q2b and Q3b. The gate bias circuits are complementary to each other and are provided by the on chip CMOS circuit shown in Figure 3.3. If 0 Volts is supplied to the gates of Figure 3.3, then “/Control” is high turning on the MOSFET Q2b. This allows current to flow from Q1a through Q2b and Q2a and thus biasing RF transistors Q1 and Q2, which provides a path for a signal on input #1 to be amplified by Q2 in a common emitter configuration and then by Q1 in a common base configuration. In addition, Qin2 is turned on to increase isolation between the “off” input #2 and the output by shorting that input to ground. When 1.5 volts is supplied to the gates of Figure 3.3, then “/Control” is low shutting off Q2b, but Q3b is
turned on allowing a signal on input #2 to be amplified and Qin1 is turned on shorting input #1 to ground. A high degree of tracking was accomplished because both sides of the “switch” were fabricated in one chip.

**Figure 0.2**: Detailed Switchable LNA
Optimizing this design for the intended application requires that RF transistors Q1, Q2 and Q3 consist of one bipolar transistor each, having their emitter stripe width fabricated at the smallest possible size to allow for the lowest possible noise figure and highest gain (See section 3.3). This option is available because high power handling is not a concern as explained in Chapter 2. Current mirror transistors Q1a, Q2a and Q3a were chosen to be bipolar transistors the same size as their counterparts to ensure proper current mirroring. The FETs Q2b and Q3b acting as switches for the current mirrors were designed with large gate widths totaling 300um to provide low resistance when turned on. Likewise FETs Q1in and Q2in were designed with the same gate widths as Q2b and Q3b to provide adequate shorting of the signal when that path is turned off. The size and performance of these active devices along with the passive devices available for this design depends on the technology used to fabricate this LNA, which will now be explained.

3.2 Technology

The most promising technology available for this project was IBM’s hybrid bipolar CMOS processes BiCMOS7HP (7HP) and BiCMOS8HP (8HP). The most
advanced CMOS process available at the time of this study was the CMRF8SF (8RF). The 8RF processes being purely CMOS, and so the cheapest, was considered first. However, the minimum 120nm FET size for the gate length is too large to provide the noise figure and gain required at 19GHz. The 7HP process is cheaper than the 8HP process with its minimum emitter width of 280nm compared to the 8HP process having 120nm, so therefore easier to fabricate. This translate to the 7HP bipolar transistor having a frequency of transition \( (f_T) \) of 120GHz compared to 8HP process capable of \( f_T = 200\text{GHz} \). Preliminary results showed that both technologies have adequate gain at 19GHz, but the 8HP was chosen because the results show it has a 0.5dB noise figure advantage over the 7HP. Resistors, capacitors, inductors, transmission lines and substrate resistivity of 14 Ohm-cm are the same in both technologies given that the same metal options are used in both processes.

### 3.2.1 Passive Components

The choice of metal options will primarily affect the inductors and transmission lines because of their dependence on return ground and the dielectric properties. The only metal option for this project was five metal layers as shown in Figure 3.4. Metal layers M1, M2 and MQ are copper whereas metal layers LY and AM are aluminum. Table 3.1 lists the electrical and physical properties for this stack.

---

1 At the time of this writing there has been significant improvement in the CMOS process that allows gate lengths down to 45nm.
Figure 0.4: Cross section showing the five metal layer option

Table 0.1: The physical and electrical properties for the 5 metal layer process option. Source: IBM 8HP Design Guidelines.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Thickness</th>
<th>Resistance</th>
<th>er</th>
</tr>
</thead>
<tbody>
<tr>
<td>AM</td>
<td>4um</td>
<td>7mOhm/Sq</td>
<td>-</td>
</tr>
<tr>
<td>Oxide</td>
<td>4um</td>
<td>-</td>
<td>4.1</td>
</tr>
<tr>
<td>LY</td>
<td>1.25um</td>
<td>23mOhm/Sq</td>
<td>-</td>
</tr>
<tr>
<td>Oxide</td>
<td>4um</td>
<td>-</td>
<td>4.1</td>
</tr>
<tr>
<td>MQ</td>
<td>0.55um</td>
<td>34mOhm/Sq</td>
<td>-</td>
</tr>
<tr>
<td>Oxide</td>
<td>0.65um</td>
<td>-</td>
<td>4.1</td>
</tr>
<tr>
<td>M2</td>
<td>0.32um</td>
<td>58mOhm/Sq</td>
<td>-</td>
</tr>
<tr>
<td>Oxide</td>
<td>0.35um</td>
<td>-</td>
<td>41</td>
</tr>
<tr>
<td>M1</td>
<td>0.29um</td>
<td>64mOhm/Sq</td>
<td>-</td>
</tr>
</tbody>
</table>

The metal option was chosen in the design kit at the beginning of the schematic entry. This sets up the appropriate physical and electrical properties for the inductors and
transmission lines in the design kit so feedback can be provided on the expected inductance, characteristic impedance, phase shift, resonance frequency and quality factor when given the metal layer and physical size of the element. Two forms of inductors are offered in this kit: inductor and rffield. The inductor option lays out a square shape coil on the AM metal layer over the choice of a resistive substrate or a lattice of metal on layer M1 to act as ground. A limited number of turns are available to achieve the required inductance. The rffield option lays out on the AM metal layer a simple straight line over a resistive substrate. Both has their advantages and disadvantages. The coil can achieve a high inductance value in a relatively small area, but the metal resistance and capacitance coupling between the coils themselves and the coils to the substrate limits its usable frequency. Rffield can achieve higher quality factor over frequency per inductance compared to inductor, but the straight line quickly takes up valuable die area. Both models calculate the inductance given the layout parameters defined by the user. Both elements require 50um clearance from all substrate contacts in the layout in order for the models to be valid. The rffield model also requires that the surrounding return ground (usually M1) in the layout was kept below 5 Ohms of series resistance. Later in this chapter and in Appendix A it will be shown that the accuracy of the rffield model was found to be more dependent on the layout than the above instructions indicated.

It was found that the inductor element’s resonance frequency was too low at the required inductance, so only rffield elements were used for this project having the high resonance at the needed inductance. Figure 3.5 provides a layout representation of the rffield inductor. The inductance and Q of this component at 19GHz varies with respect to its length. Some examples are a 10um wide 200um long device has an inductance of
178pH and a Q of 40. A 10um wide 400um long device has an inductance of 410pH and a Q of 31. And a 10um wide 600um long device has an inductance of 650pH and a Q of 17.

**Figure 0.5:** Inductor rfname

The transmission line element called `singlewire` required entry of the metal layer for ground return. The model outputs the characteristic impedance, phase delay and loss for the given metal width and length. Having side ground shields is an option that improves noise immunity. For this project, all transmission lines had side shields with the signal layers done on the AM metal over M1 to provide the lowest resistance loss. The limitation of `singlewire` is that its model only applies for straight paths. All turns and tees had to be simulated using the extraction tools, which will be explained later in this chapter. Figure 3.6 shows a layout representation of the transmission line `singlewire` with the optional side shields. The side shields are connected to the ground wire in metal layer M1 through via connections. Note that the ground metal on M1 is laid out in stripes running parallel with the transmission lines to meet layout design rules. These ground metal stripes cover the full area under the transmission line and side shields.
Figure 0.6: Transmission line *singlewire*

All capacitors in the design are metal-insulator-metal (MIM) capacitors because they offer higher Q and less coupling to the substrate noise than their MOSCAP counterparts. The MIM capacitor is formed by two metal plates on layer QY over LY with dielectric in between. Note: QY is not shown in figure 3.4 because this is not a signal layer. The model indicates capacitance for a given length and width. Capacitor coupling to the substrate is taken into account by the model.

Two types of resistors were used in this design: *oppcres* and *opndres*. The *oppcres* has resistance rating of 254 Ohm/sq with a 20% tolerance. These were used for the 7.5kOhm resistors biasing Q2, Q2a, Q3 and Q3a. The *opndres* resistor has a rating of 72 Ohm/sq with a 10% tolerance. These were used for the remaining resistors which required less than 500 Ohms. The given tolerance is dependent on the doping variation of the process and not the variation in physical size of the process, so choosing the resistor technology according to the resistor value allowed larger sizes, which decreased the effect that physical variation had on total resistance.

The bondpads were designed to accommodate ribbon wire. The smallest dimension allowing ribbon bonding was 100um by 90um. These elements have
capacitance to the substrate because of their size. In order to reduce this coupling, there are two options to apply underneath the pad: a lattice of P+ polysilicon (PC), or a region of N+ subcollector (NS). Selecting the PC option in the model shows a 41.4fF capacitance in series with a 7.2 Ohm resistor to the substrate compared to 41.4fF capacitance in series with a 6.3 Ohm resistor for the NS option at 19GHz. The NS option was used for this design.

The 8HP technology offers ESD devices for the IO and supply ports. The disadvantage of ESD devices is that they are capacitive to the substrate so substrate noise is induced. The substrate having low resistance also loads down the IO ports which increases noise figure with increase in frequency. For comparison, two designs were done with one containing ESD protection and the other with none. The design without the ESD is named LNA1 and the design with ESD is named LNA2. In addition to the ESD devices, LNA1 and LNA2 were laid out differently for reason of application as explained later in this chapter.

The key component in this technology that performs the amplification of the signal is the “heterojunction” bipolar transistor. The designer can choose a range of sizes and single or dual emitter stripes for this component depending on application. The next section examines the electrical properties of this transistor. These properties govern the DC biasing and matching required for stability, gain and noise figure for this application.
3.2.2 HBT: Biasing and Sizing

Choosing the DC biasing of the transistors in this circuit requires consideration of the voltage breakdown of the transistors and the collector current to achieve required noise and gain for the size of the transistor.

The junction voltage breakdown for the high performance transistor is shown in Table 3.2. It will be shown later that this design places stress mostly on the collector to emitter voltage parameter. The other junctions are biased well below the limits.

Table 0.2: Electrical Limits for the High Performance HBT

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Units</th>
<th>Minimum</th>
<th>Nominal</th>
<th>Maximum</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BE}$</td>
<td>Volts</td>
<td>0.696</td>
<td>0.726</td>
<td>0.756</td>
<td>$I_C = 10 \mu A, V_{CB} = 0$</td>
</tr>
<tr>
<td>Beta</td>
<td></td>
<td>100</td>
<td>600</td>
<td></td>
<td>$V_{BE} = 0.72 V, V_{CB} = 0$</td>
</tr>
<tr>
<td>$f_T(peak)$</td>
<td>GHz</td>
<td>180</td>
<td>200</td>
<td></td>
<td>$V_{CB} = 0.5 V, I_C = 12 mA/\mu m^2$</td>
</tr>
<tr>
<td>BVCEO</td>
<td>Volts</td>
<td>1.5</td>
<td>1.77</td>
<td></td>
<td>$I = 10 \mu A$</td>
</tr>
<tr>
<td>BVCSO</td>
<td>Volts</td>
<td>20</td>
<td>50</td>
<td></td>
<td>$I = 10 \mu A$</td>
</tr>
</tbody>
</table>

Gain and noise is dependent in part on $f_T$. The SiGe doped base and the smaller emitter stripe width increases $f_T$ by reducing the transient time through the base, the base resistance, and the collector capacitance [11]. These same properties that increase $f_T$ also reduce the minimum noise factor ($F_{min}$) according to the linear equation 3.1 [12].

$$F_{min} = 1 + \frac{1}{\beta} + \frac{n \cdot gm \cdot rb}{\beta} + n \cdot gm \cdot (re + rb) \left( \frac{f}{f_T} \right)^2 +$$
where \( f_T = 1/(2\pi \tau) \), \( \tau \) is the total forward transient time through the transistor, \( r_b \) is the total base resistance and \( r_e \) is the emitter resistance, \( \beta \) is the common emitter current gain, \( g_m \) is the transconductance and \( n \) is the junction grading factor ranging from 1 to 1.2. Equation 3.1 can be simplified because Table 3.2 shows that \( \beta \) is large and \( r_b > r_e \). Also, \( f_T \) is much higher than 19Ghz. This simplification is given in equation 3.2 using \( g_m = qI_c/(kT) \) and assuming \( n = 1 \).

\[
F_{\text{min}} = 1 + \sqrt{\frac{2qI_c r_b}{kT} \cdot \left( \frac{1}{\beta} + \left( \frac{f}{f_T} \right)^2 \right)}
\]

(3.2)

\( r_b \) can be reduced by increasing the length of the emitter stripe, which would reduce \( F_{\text{min}} \), but higher collector current is required to increase \( g_m \) to maintain a high \( \beta \) offsetting some of the benefit. How much benefit to noise reduction, if any, must be determined. It is also important to analyze \( r_b \) for matching purposes. Using table 3.3, the optimal emitter length for base matching was expected to be between 3um and 12um.
To verify this, the HBT was characterized with respect to size and the collector current (Ic). A collector voltage of 1.25 volts was used to ensure reverse bias of the collector to base junction. Three sizes of transistors were simulated with respect to Ic to compare Rb. Figure 3.7 and 3.8 compares the base resistance and reactance with respect to Ic for three emitter stripe sizes: 120nm x 3um, 120nm x 8um and 120nm x 12um. Figure 3.7 shows that the base resistance at 19GHz increases with Ic, particularly with the smallest device. It is expected that the base resistance increases due to DC charge crowding out the higher frequency charges due to the skin effect. The simulated base resistance in figure 3.7 compares closer to the extrinsic base resistance in table 3.3. The base reactance in figure 3.8 moves closer to zero with increase in Ic because the depletion layer width decreases causing capacitance to increase.
Figure 0.7: Input Resistance ($r_b$) vs. Emitter Stripe Size and Collector Current.

Figure 0.8: Input Reactance ($x_b$) vs. Emitter Stripe Size and Collector Current.

The DC collector current also determines gain and noise performance. Again, three sizes were compared with respect to the collector current. The maximum stable power gain ($G_{msg}$) is graphed in figure 3.9, and the graph for minimum noise figure is
shown in figure 3.10. The gain increases with $I_c$ because it is related to $f_{\text{max}}$, which is dependent on $f_T$, which is proportional to the transconductance ($g_m$) [11]. This dependence of $f_T$ on collector current is shown in figure 3.11. More current is required to reach the same $f_T$ as the emitter stripe length increases because $g_m$ needs to overcome the larger base to emitter and base to collector capacitance. It can be seen that $f_T$ and $G_{\text{msg}}$ peaks and then rolls off due to the Kirk effect [11]. The graph in figure 3.9 shows that the gain of 20.5dB can be obtained for all three size transistors because of the tradeoffs between decreases in base resistance to the increase in base to collector capacitance with increases in the emitter length. The optimal collector current for gain for the 120nm x 3um size emitter stripe is 6mA, for the 120nm x 8um is it 14mA and for the 120nm x 12um it is 24mA. The advantage of using a large device is it can handle more DC current resulting in an increased IP3, but radiometers such as this one do not require large IP3.

Decreasing $r_b$ was not enough to reduce $F_{\text{min}}$ as can be seen in the noise graph of figure 3.10. Increasing the emitter stripe from 3um to 8um increases the $F_{\text{min}}$ by 0.01dB. Increasing it from 3um to 12um increased the $F_{\text{min}}$ by 0.03dB. The graph also shows that $F_{\text{min}}$ decreases and then increases with increase in collector current. The noise figure starts high because gain is low, then it decreases to a minimal as gain increases until the increasing DC current causes the thermal and shot noise to outpace the benefit of the increasing gain. The optimal collector current for $F_{\text{min}}$ for the 120nm x 3um size emitter stripe is 500uA, for the 120nm x 8um is it 1.5mA and for the 120nm x 12um it is 2.0mA. The expected operating $I_c$ range for a given size transistor will be between its minimal noise figure and maximum gain.
Figure 0.9: Maximum 19GHz Signal Gain vs. Emitter Stripe Size and Collector Current.

Figure 0.10: Minimum 19GHz Noise Figure vs. Emitter Stripe Size and Collector Current.
Another important consideration in choosing transistor size and collector current is the sensitivity of the noise figure of the transistor with respect to input match. How noise figure changes with the input match is given in equation 3.3 [13].

\[
f = f_{\text{min}} + \frac{m}{g_s} |y_S - y_{\text{opt}}|
\]  

(3.3)
where \( r_n \) = normalized equivalent noise resistance, \( g_s \) is the normalized source conductance, \( y_s \) is the normalized input reflection coefficient and \( y_{\text{opt}} \) is the normalized input reflection coefficient that gives \( f_{\text{min}} \). This equation shows that the sensitivity depends on the equivalent noise resistance \( (R_n) \). The dependence of \( R_n \) on \( I_c \) and size is given by equation 3.4 when using the same assumptions given for equation 3.2 [12].

\[
R_n = \frac{kT}{2qI_c} + r_b
\]  

(3.4)

Figure 3.12 along with table 3.3 confirms equation 3.4. The graph shows that the 120nm x 3um transistor has an \( R_n \) of \( >300 \) Ohm at low collector current, then drops to 80 to 90 Ohm as \( I_c \) increases leaving \( R_n \approx r_b \). As expected at higher \( I_c \), the other two sizes \( R_n \) compare to their \( r_b \), which is in the 25 to 35 Ohm range.

![Figure 0.12: Equivalent Noise Resistance at 19GHz with respect to emitter stripe size and \( I_c \).](image-url)
Equation 3.3 also indicates that that the input match needs to be considered for noise figure. Again the same three transistor sizes were compared with respect to \( I_c \). The results are shown in figure 3.13. As the collector current increases, the optimal match moves toward the center for all three sizes. The 120nm x 3um emitter stripe transistor has an optimal match in the vicinity of (300+j100) Ohm compared to (100+j50) Ohm for the 120nm x 8um transistor and (75+j30) Ohm for the 120nm x 12um transistor.

**Figure 0.13:** Optimal Input Match at 19GHz with respect to emitter stripe size and \( I_c \).

Matching the input for the maximum gain would be the complex conjugate of the input impedance given in figures 3.7 and 3.8. The approximate match for the 120nm x 3um transistor is 48+j200 Ohm, 20+j50 Ohm for the 120nm x 8um transistor, and 15+j20 Ohm for the 120nm x 12um transistor. Matching for minimal noise figure for the 120nm x 3um transistor would have a magnitude reflection coefficient of 0.75. The next size up would have a magnitude of 0.66 and the largest transistor would have a magnitude of 0.68. These plots will shown to be accurate later in this section.
Taking all of above factors into consideration, the transistor size chosen for this design has an emitter size of 120nm x 8um biased with a collector current of 4.5mA. This size sets the base resistance closer to 50 Ohm according to table 3.3 but 20 Ohm according to figure 3.7. The collector current of 4.5mA allows a low minimal noise figure of 1.3dB while maintaining adequate gain: $G_{msg} = 18.4$dB. Having a Zopt of 100+j30 Ohm and an Rn of 35 Ohm makes it easier to match and less sensitive to mismatch compared to the smaller transistor. Another advantage of using a larger transistor is process variation would have less effect. Using a transistor larger than 120nm x 8um would require more power then necessary and matching would be more difficult because the low input impedance.

With the size and collector current set, a Gummel plot was made to determine the base current (Ib) and base to emitter voltage (Vbe). The plot indicates that a base current of 12 uA is drawn with a Vbe of .87mV. Setting the collector to emitter voltage (Vce) was determined from plotting Vbe verses Vce with a forced base current of 12uA. The point on the graph where Vbe intersects Ib has a Vce of 1.125 volts. The transistor was then setup with this bias and had its collector, base and emitter impedance characterized with respect to frequency so a matching circuit could be designed; this include matching the node connecting Q1, Q2 and Q3 shown in figure 3.2. Matching this node and the I/O ports is discussed next.

### 3.3 Matching

Now that the size, biasing and s-parameters have been determined for the single HBT, the switching cascode shown in figure 3.2 was setup in a schematic tool, Cadence Composer, except for the matching circuits, the ESD circuits and the I/O pads. All
components had associated models. A supply voltage of 2.25 volts was chosen to provide approximately 1.125 volt drop across each of the transistors. An iterative approach was done in setting up the resistor values and gate lengths of the FETs until appropriate dc voltage and currents were obtained. High resistor values of 7.5k Ohm were used for biasing the bases of Q2 and Q3 to prevent input signal loss to the resistor. A total gate length of 300um was required for the FETs to keep the channel resistance less than 40 Ohm to ensure a small DC voltage drop. S-parameters were taken to evaluate stability, noise, gain and isolation. |S22| was >0dB so negative feedback between collector and base on Q1 was required to make conditional stability. Isolation and gain was improved by designing transmission lines to act as an impedance transformation between Q1, Q2 and Q3 so the “off” transistor, say Q3, would look more like an open and Q1 would better match the “on” transistor, Q2 and vice versa. This was accomplished by evaluating the collector impedance of Q2 (Q3 is the same) when it was on and off and the emitter impedance of Q1 (always on). Transmission lines were designed as 50 Ohms and took into consideration these transistor impedances and the frequency phase shift with respect to its length.

The collector output impedance of the common emitter stage when it is on is (159-j103) Ω. The negative reactance is in large part due to the collector-base capacitance. This capacitance results in the Miller effect that can be shifted to become real and add to the input resistance by adding a degenerate emitter inductor [14]. The advantage of doing this is to increase input resistance to improve matching and stability without degrading the noise performance [15]. Improving input match helps bring zopt closer to optimal input gain match. Too much inductance decreased gain because the
signal voltage on the emitter increases causing negative feedback. An optimal degenerate inductor value of 117pH was determined by comparing noise, stability, gain and match. This much of the circuit was then laid out in Cadence Virtuoso and verified to the schematic. Extraction was done to include the added parasitic components of the layout including the transmission lines, then re-simulated to compare to the schematic results to ensure that there were no major changes.

The stability, gain, and noise circles representing the core of the cascode layout are shown in figures 3.14 through 3.17. Figure 3.18 show the $|S21|^2$ gain at 19GHz. Figure 3.14 show that the source stability circles for 10 to 40GHz lies outside of the smith chart. The load stability circles however do lie in the smith chart as shown in figure 3.15, so it is not possible to simultaneously match both input and output ports.

The matching circuits for both input and output port had to include the I/O pads and bondwire (for LNA1) as shown in figure 3.19. The bondwire value of 150pH was determined by methods explained in Appendix B. The inductor used to match the output also provide the DC current to this circuit and is AC shorted to ground on the DC supply side using 5pF of capacitance (not shown). The matching component values used for the matching depended on the results of the extraction technique used on the layout. The extraction techniques are explained in Appendix A. Using the ‘rlck’ extraction technique resulted in the optimal output matching consisting of two series 114fF capacitors in shunt with a 588pH inductor. The result of output match seen by the collector of Q1 is plotted as $Z_{load}$ in figure 3.15 to show that it does not enter any of the load plane stability circles and thus will not produce an $|S11| > 1$. 
In addition to stability, the chosen output matching component values provides a high gain, but with enough margin below the maximum stable gain to ensure stability against process variations. This is proven by mapping the output match shown in figure 3.15 to the power gain circles resulting from load mismatch shown on the right of figure 3.16. This plot indicates a power gain at 19GHz to about 20dB marked by M2.

The noise circles plotted in figure 3.17 show that a noise figure of less than 2.25dB is possible. Adding the degenerate inductor shifted the optimal match to (40+j150)Ω from that of (100+j50)Ω that was shown in figure 3.13. This shift also moved it closer to the center of the available gain circles for the given load as shown in figure 3.16. The noise circle plot also shows what the input, base of Q2, should see looking back at the matching circuit when comparing the schematic to the extracted results; legend as Schematic and Layout (rlck) respectfully. There were problems getting the layout match to move closer to the center of the noise and gain circles. The only two component matching circuit with reasonable valued components consisted of 140 fF capacitor and a shunt 440pH inductor looking in from the I/O pad. To shift the match closer to the center of the noise circle would have required making the capacitor smaller. This solution proved to have higher losses increasing the noise figure. It was decided to leave the match as is because the noise circles indicate 2.5dB noise figure and a transducer power gain of 18.5dB as indicated by marker M1 in figure 3.16.
Figure 0.14: Source Stability Circles for 10GHz to 40GHz.

Figure 0.15: Load Stability Circles for 10GHz to 40GHz. Zload is the load that the LNA sees at its output.
Figure 0.16: Available and Power Gain Circles for 19GHz. Available gain circles (16dB, 18dB, 18.5dB, 19dB, 20dB in center). Power gain circles (14dB, 16dB, 18dB, 20dB).

Figure 0.17: Noise Figure Circles at 19GHz.
Figure 0.18: \(|S21|^2\).

Figure 0.19: Matching Circuits

3.4 Layout

Figure 3.17 showed how the input matching shifted when the parasitic elements of the layout were included. The output match shifted as well but it was compensated by changing values of the matching components. Also, the ESD devices were not
considered. These devices will also load down the I/O ports. How much loading at 19GHz was not well known so there were two designs fabricated: LNA1 and LNA2.

3.4.1 LNA1 Layout

LNA1 was designed for optimal performance with respect to frequency by designing it without ESD protection to avoid loading of the I/Os. The input ports were placed opposite of each other on the die and orthogonal to the output port to maximize isolation. The layout for LNA1 is shown in figure 3.20. The dimensions are 1.83mm by 1.13mm.

Pre-layout simulations were done in the schematic using the models available from the design kit to determine the power supply, and what type of transistor and size would be required to deliver the needed performance listed in chapter 2. These simulations also determined if it was feasible to use on chip passive components for the matching, including the bond wires.

There are a number of items in the layout that require attention when designing for the K-band to ensure the final results from the layout closely match those from the schematic. Post layout simulations had to be done to take into account the parasitic elements induced in the layout. The effect that these parasitic elements had on the schematic design and the required changes to the design to compensate for them is discussed later in this chapter.
Figure 0.20: LNA1 Layout

Figure 3.20 shows that each signal pad has a ground-signal-ground (GSG) configuration for improved transition of the EM field propagating between the die and the bond wires or test probes. Not easily seen in figure 3.20 is that the signal pads are tapered down to the transmission line width for additional improvement in transition. These pads were place on a 125um pitch governed by the test probes available for the required test frequency. The supply pads and the control pad have their own tightly coupled ground pad to ensure proper ground return. Each of these pair of pads was also done at a 125um pitch.

The signal paths were done on the thickest metal AM level, since it has the lowest cross-section resistance to reduce loss and since its larger distance from the substrate.
reduces noise coupling. The transmission lines that are greater than 100um in length had side shield added to reduce coupling to other devices and metal wires. The paths were kept as straight as possible from the input pad through the matching circuits, through the common emitter stage, Q2 or Q3, onto the emitter of Q1. Likewise, the path from the collector of Q1 to the output pad was laid out straight. This was done to reduce reflections. The line lengths from the input pads to the common emitter stages are 135um. The line lengths from the common emitter stages to the common base stage are 293um and the line length from the common base stage to the output is 458um for a total of 886um.

Connecting the top metal to the transistors had to be made through vias. These vias were placed as close as possible to the transistor’s ports and kept as wide as the AM metal and to keep losses low and maintain good transitions. All transitions to the transistors were tapered to reduce reflections. Tapers were also used when metal widths had to change.

Figure 3.21 shows more detail around Input1. The ground plane M1 has been removed for clarity. The references correspond to those shown on the schematic in figure 3.2. One item worth noting in this layout is the placement of components. The input pad, the matching capacitor, the matching inductor, Qin1 and Q2 are placed as close as possible to minimize the interconnect effects on the models simulated in the schematic. The matching capacitor and inductor being tied to the base of Q2 has a DC voltage applied to them, so the capacitor also functions as a DC block to the input pad and the matching inductor has capacitors totaling 5pF tying its end to ground, acting as a short at the operating frequencies.
Figure 0.21: Matching Circuit for Input 1

The current mirror transistor Q2a, being the same type and size as Q2 to ensure better current mirroring, was placed in close proximity of Q2 to better insure equal fabrication of the two and to insure equal resistance in their DC biasing. These components can be seen in figure 3.20. Another critical component shown in figure 3.20 and figure 3.21 is the degenerate inductor. It is kept as close as possible to Q2 emitter to ensure minimal impact the interconnection has on the model. This inductor, like all the inductors is modeled by the design kit. The model of the inductor was verified using Agilent’s ADS layout tool, and then simulated using Agilent’s ADS tool Momentum. The return current on the substrate and the nearby metal layer M1 was taken into consideration. The Momentum results were compared to the schematic kit model to ensure minimal impact to the final extraction simulation results. These results and the simulation results are discussed in chapter section 3.5.
3.4.2 LNA2 Layout

LNA2 was designed for the application including ESD protection. The application required that the input ports to be placed in the top left corner with respect to the output located in the lower center of the right side of the die. The control functions and supply had to be placed in the upper right side of the die. The layout for LNA2 is shown in figure 3.22. The dimensions are 1.71mm by 1.20mm.

Figure 0.22: LNA2 Layout

The same attention to placement was done for this layout as for LNA1. The GSG pads were placed at 125um pitch. The biasing transistors were place close to the amplifying transistors to ensure equal fabrication. There are three differences between
the two layouts in addition to the I/O placement. They are; the addition of ESD components, the absence of the component singlewire, and the total transmission line length is 1751um for Input1 and 1684um for Input2 compared to 886um for both inputs of LNA1. The ESD components are identified in the figure. The ESD components on the transmission lines and VC control I/O are low capacitance double diodes circuits. They are low loading and require that the signal may not exceed the power supply. The latter is not a problem for this circuit. The ESD component for the CMOS I/O is a bipolar base power clamp. A variable triggered power clamp ESD circuit was required for the higher voltage supply of VCC, but this was not available in the design kit at the time of fabrication. The transmission line lengths from the input pads to the common emitter stages are 193um, which is 58um longer than those for LNA1. The transmission line lengths from the common emitter stage Q2 to the common base stage Q1 is 292um and for Q3 to Q1 it is 225um. The transmission line from Q1 to the output is 1231um. Comparing these line lengths to LNA1 shows that the majority of transmission line difference lies in the output line: 1231um compared to 458um. The same matching topology was used for LNA1 is used for this design.

Post layout simulations for LNA2 were done similar to LNA1 as described in the previous section. The effect that the parasitic elements had on the schematic design and the required changes to the design to compensate for them is discussed later in section 3.5.4.
3.5 Post Layout Simulations

In the following subsections we describe post layout simulations of; the inductors, the DC response, stability, S-parameters and noise figure, and transient response.

3.5.1 Model vs. Extraction vs. EM simulator: an Inductor Analysis

The inductor model in the schematic is documented to be accurate if the return current in the layout sees less than 5 Ohm resistance and any substrate contacts, placed by the designer, are at least 50um away from the inductor metal line. Substrate contacts are typically used to electrically connect the substrate to the designer’s defined ground metal. The rfline design generated in the layout called a pcell, requires an added shape in the layout tool called BB IND to surround the ground node of the inductor end to the designers defined AC ground metal, M1 metal in this case, so proper post layout extractions can be performed. A layout was built using Agilent’s ADS tool to confirm the accuracy of these models and to prevent major layout changes due to considerable differences between the final extraction results and the schematic simulations. ADS has a simulator called Momentum that is a “2.5” dimensional EM simulator that requires the physical and electrical properties of the dielectric and metal stack-up. These properties are taken from the IBM Design Manual. A test case was done on the 440pH inductor that is used to match the input. Adding the 5pF of capacitance to one end this inductor to tie it to ground will ideally have this circuit looking like a 426pH inductor. The inductor was drawn in the layout tool of ADS at a length of 477um and a width of 9um on the top metal AM to match that in the chip layout. Two ground planes drawn around it 60um away on metal layer M1 similar to what was done in the design layout. A 50 Ohm port was connected to each end. The two port s-parameter file was imported into the
schematic tool. One port was connected to ground through 5pF of capacitance and the resulting one port simulated. The S11 result was (0.25+j47) Ohms. The imaginary part of 47 Ohm equates to 394pH at 19GHz; 32pH less than the ideal 426pH. This experiment was repeated, simulating the equivalent schematic components and for the layout using the “rlck” extraction method. The schematic simulated 403pH and the layout simulated 396pH. After considering the 5pH MIM capacitors, both results from Momentum and the Assura extraction indicates that the inductor is approximately 410pH, 6.8% less than the 440pH predicted by the rfline model. This difference is expected to result from the added ground metal laying under the inductor ends. Therefore the “rlck” extraction method in conjunction with the rfline model was taken to be accurate for this design. However, it is shown in Appendix A that this layout was optimal for the accuracy of the rfline model.

3.5.2 DC Analysis for LNA1 and LNA2

The matching components and the I/O pads were added to the layout as shown in figure 3.20 for LNA1 and figure 3.22 for LNA2. The extraction methods explained in Appendix A were performed and compared to the schematic. The first simulation performed was to verify DC biasing. DC analysis of the four extraction methods, RC, RLCK, PEEC and LADDER are compared to the schematic simulation and given in table 3.5. Only the RLCK extraction method was done for LNA2. Results show that all extraction methods create a current model that draw less supply current than the schematic model, with the “RC” and “PEEC” modeled circuits drawing the least.
Table 0.4: DC Analysis for LNA1 and LNA2.

Voltage Supply = 2.25VDC, CMOS Supply = 1.5VDC, VC=1.5VDC (RFin 1 on)

<table>
<thead>
<tr>
<th>Simulation</th>
<th>Current Supply</th>
<th>CMOS Supply</th>
</tr>
</thead>
<tbody>
<tr>
<td>Schematic (LNA1 and LNA2)</td>
<td>9.16mA</td>
<td>47.6nA</td>
</tr>
<tr>
<td>&quot;RC&quot; (LNA1 Only)</td>
<td>8.84mA</td>
<td>47.6nA</td>
</tr>
<tr>
<td>&quot;RLCK&quot; (LNA1 and LNA2)</td>
<td>8.915mA</td>
<td>47.6nA</td>
</tr>
<tr>
<td>&quot;LADDER&quot; (LNA1 Only)</td>
<td>8.915mA</td>
<td>47.6nA</td>
</tr>
<tr>
<td>&quot;PEEC&quot; (LNA1 Only)</td>
<td>8.82mA</td>
<td>47.6nA</td>
</tr>
</tbody>
</table>

Voltage Supply = 2.25VDC, CMOS Supply = 1.5VDC, VC=0VDC (RFin 2 on)

<table>
<thead>
<tr>
<th>Simulation</th>
<th>Current Supply</th>
<th>CMOS Supply</th>
</tr>
</thead>
<tbody>
<tr>
<td>Schematic (LNA1 and LNA2)</td>
<td>9.16mA</td>
<td>162nA</td>
</tr>
<tr>
<td>&quot;RC&quot; (LNA1 Only)</td>
<td>8.81mA</td>
<td>162nA</td>
</tr>
<tr>
<td>&quot;RLCK&quot; (LNA1 and LNA2)</td>
<td>8.91mA</td>
<td>162nA</td>
</tr>
<tr>
<td>&quot;LADDER&quot; (LNA1 Only)</td>
<td>8.91mA</td>
<td>162nA</td>
</tr>
<tr>
<td>&quot;PEEC&quot; (LNA1 Only)</td>
<td>8.81mA</td>
<td>162nA</td>
</tr>
</tbody>
</table>

3.5.3 Stability Analysis for LNA1 and LNA2

The second simulation performed was for stability. Figures 3.23 and 3.24 show two stability measurements versus frequency for LNA1. The first figure shows that the Rollett’s stability factor is greater than 1. The second figure plots $|\Delta|$ and shows a magnitude less than 1. Together these two results indicate an unconditionally stable circuit. Both plots include the 150pH bondwires, but removing the bondwires did not change stability.

The same stability analysis was performed for LNA2. The results were similar to that for LNA1 in that the Rollett’s stability factor is greater than 1 and $|\Delta|$ was less than 1. The core layout was shown to be potentially unstable so the added loss from the matching circuitry and bondpads increased both layouts stability to be unconditional.
3.5.4 S-Parameter and Noise Figure Analysis for LNA1 and LNA2

After ensuring stability, three port S-parameter and noise analysis was done to compare ports: Input#1, Input#2 and Output. It had to be done four times for LNA1;
twice when Input#1 was on (Input#2 was off) with and without the 150pH bondwires, then twice again for the opposite mode to ensure duality. LNA2 was simulated without bondwires since its matching circuitry was designed to match directly to 50 Ohms. The reason for this is that it was discovered that the 150pH inductor models were disabled during simulations, and the time to do two layouts proved too short to make changes before submission to fabrication. All of the four extracted models were simulated for LNA1. Only the ‘rlck’ extracted model results are discussed in this chapter because it was considered accurate. The plots showing the results for all of the four extracted models are shown in Appendix C for LNA1. Only the ‘rlck’ extracted model was simulated for LNA2. All results were tabulated in this chapter for easy comparison.

The first plot analyzed is the gain. Supplying 1.5 volts to port “VC” turns the current mirror on for Input#1 and shorts the input for Input#2. Supplying 0 volts to port “VC” reverses the states. Both conditions were simulated and the gains for both inputs for LNA1 were overlaid in the plot shown in figure 3.25. The “rlck” gain peaks at 18.7dB for Input#1 and 19.1dB for Input#2. Both are within 0.5dB of each other and have a gain variation of less than 0.15dB in the operating bandwidth. This gain falls in the middle of the expected 18dB to 19dB gain and exceeds the gain specification in magnitude and flatness. As mentioned previously, the match was tuned based on the “rlck” extractions. The gain simulated for the other extracted models are compared to each other for LNA1 in Appendix C. Running a temperature analysis showed that the gain increases with temperature at a rate of 0.01dB/˚C. The expected gain when testing the die without the matching bondwires is shown in figure 3.26. Here the peak gain
dropped by 0.9dB for Input#1 and 0.85dB for Input#2 when comparing the “rlck” extracted model.

The two inputs for LNA2 gain is plotted in figure 3.27. It shows that the expected gain for wafer probing will peak at 15.90dB for both inputs at 18.25GHz. The flatness across the band is 0.3dB. The two input gains are closer to each other than those for LNA1 because the input matching capacitors and inductors for the two inputs were changed with respect to one another. The required change to achieve identical gain was less than 5 fF for the capacitors and 5pH for the inductors. This is also indicated in the input reflection plots soon to be discussed.

![Figure 0.25](image.png)

**Figure 0.25**: LNA1, Input#1 and Input#2 to Output gain including the 150pH wirebonds
Figure 0.26: LNA1, Input#1 and Input#2 to Output gain without wirebonds.

Figure 0.27: LNA2, Input#1 and Input#2 to Output gain without wirebonds.

Figure 3.28 is a plot comparing the noise figure for Input#1 and Input#2 of LNA1.

The expected noise figure is 2.78dB for Input#1 and 2.64dB for Input#2. This is 0.3dB
higher than that simulated using the schematic model because of added losses due to the parasitic components themselves. Removing the bondwires raises the expected noise figure for LNA1 to between 2.9dB to 3.0dB at 19GHz as shown in figure 3.29. The expected noise figure is much lower than the target noise figure of 4.15dB.

LNA2 expected noise figure for both inputs are shown in figure 3.30. The simulation indicates both inputs are expected to 2.8dB noise figure. This design also meets the required noise figure.

![LNA1 Noise Figure Comparison between Input1 and Input2 with 150pH Wirebonds Included](image)

**Figure 0.28:** LNA1, *Input#1* and *Input#2* to *Output* noise figure including the 150pH wirebonds.
Figure 0.29: LNA1, Input#1 and Input#2 to Output Noise Figure without the wirebonds.

Figure 0.30: LNA2, Input#1 and Input#2 to Output Noise Figure without the wirebonds.

Figures 3.31 and 3.32 are plots of LNA1 inputs and output reflection coefficient respectively which include the matching bondwires. The associated plots without the bondwires are located in the Appendix B. The input match is resonant at 18GHz instead
of 19GHz because it was matched for noise. The output “rlck” match is shown to be matched at the center of the operating frequency. This match doesn’t change if Input#1 is on or if Input#2 is on. Both input and output match passes the return loss criteria.

Figures 3.33 and 3.34 are plots of LNA2 inputs and output reflection coefficient respectively. Like LNA1, the input match is resonant at 18GHz instead of 19GHz because it was matched for noise. The output “rlck” modeled match is shown to be matched at the center of the operating frequency. Both input and output match for this design passes the return loss criteria.

Figure 0.31: LNA1, Input#1 and Input#2 reflection coefficient magnitude response with wirebonds included.
Figure 0.32: LNA1, Output reflection coefficient magnitude for when Input#1 is on and when Input#2 is on. Both include the 150pH wirebonds.

Figure 0.33: LNA2, Input#1 and Input#2 reflection coefficient magnitude response.
Isolation between \textit{Input\#1}, \textit{Input\#2} and \textit{Output} was analyzed next. The first isolation analyzed was from the output port to the active input. Simulations indicate a worse case of 42dB isolation for LNA1 and 45dB for LNA2, which is sufficient in preventing changing load impedance affecting the input match. Figures of these simulation graphs along with the following isolation graphs can be found in the appendices. The next isolation analyzed was the gain from \textit{Input\#1} (active) to \textit{Input\#2} (inactive). Simulation shows an isolation of better than the specified 38dB for the operating bandwidth and decreases to 35dB out of band for both designs. This was excepted because the off port is not performing any function. A more critical isolation is required from the “off” input port to the other two ports. Simulations of the isolation between the “off” port to the “on” port is better than 54dB for both designs. The other scenario is the isolation between “off” port to \textit{Output}. The simulation results indicates that the expected isolation to be better than 30dB for both designs. This is 5dB
higher than desired, but it is acceptable at 30dB considering the high 18dB gain on the
“on” input will differentiate that signal from the “off” signal on this port by 48dB.

The reverse isolation from the output to the inactive input is high as expected with
a cascode configuration and this port is off. The isolation is expected to be better than
60dB for both designs.

For simplicity, tables’ 3.6 and 3.7 were created to compare the duality of the
LNA1 design. These tables list only the “rlck” responses having the matching wirebond
included and without it in the form of xx.xx/yy.yy respectfully. Tables’ 3.7 and 3.8 were
created to compare the duality of the LNA2 design. It is formatted like the tables for
LNA1 except no wirebond simulations were included because the matching circuitry was
optimized for 50 Ohm terminations.

Table 3.6 compares the LNA1 inputs with respect to the output having the 150pH
wirebonds for matching. The most important criteria is gain and noise figure. Simulation
shows there is an expected 0.35dB difference in their gain and 0.15dB difference in their
noise figure with Input#2 having the better performance of the two. The input reflections
for the two ports indicate a difference in their match given the 1.29dB delta. It was
expected that the difference in their match was due to the slight differences in their DC
biasing considering that both input circuitries, including their matching components, are
copies of each other. Tweaking “VC” and “CMOS” to get the biasing for both
configurations to be within 0.0001 accuracy was tried to improve this, but the gain and
noise shifted together so there was no improved correlation. The matching for Input#2
was setup to match Input#1 without the wirebonds. Adding the wirebonds magnified the
differences between the two inputs but the design was already submitted to fabrication
and so it was too late to make adjustments. Comparing isolation and the output match when *Input#1* is active to when *Input#2* is active are in good agreement.

Table 3.7 compares the isolation between the inputs. The simulation results for both inputs exceed the required isolation. The 5dB difference between the 75dB and 80dB simulation result is not a concern given the high isolation.

Comparing LNA2 tables’ 3.7 and 3.8 with LNA1 tables’ 3.6 and 3.7 shows that the gain for LNA2 will be approximately 3dB less than LNA1. The expected noise figure is 0.2dB higher for LNA2. Both LNA1 and LNA2 have the same optimized input match with LNA1 having the lowest return loss of -17.5dB at 17.7GHz (*Input#2*), and LNA2 having -17.0dB at 17.75GHz. However, LNA1 achieves a 7dB better return loss for the output match at 19GHz.

Analyzing the matching between the two layouts, the lower gain and slightly higher noise figure for LNA2 questions the accuracy between the extracted transmission lines used in LNA2 and the *singlewire* components used in LNA1; the ~ 800um difference in total lengths between the two layouts is not enough to account for the 3dB difference. This is discussed more in chapter 5.

### Table 0.5: LNA1 input ports comparison in relation to the output

<table>
<thead>
<tr>
<th>Simulation @ 19GHz (dB)</th>
<th>Input 1 (on)</th>
<th>Input 2 (on)</th>
<th>Input 1 (off)</th>
<th>Input 2 (off)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (Input to Output)</td>
<td>18.79/17.8</td>
<td>19.14/18.5</td>
<td>-29.98/-31.74</td>
<td>-29.65/-31.48</td>
</tr>
<tr>
<td>NF</td>
<td>2.79/2.96</td>
<td>2.63/2.88</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>Isolation (Output to Input)</td>
<td>42.94/44.62</td>
<td>42.64/44.48</td>
<td>60.93/62.82</td>
<td>61.24/63.12</td>
</tr>
<tr>
<td>Input Reflection Coefficient</td>
<td>-14.75/-6.77</td>
<td>-13.25/-6.34</td>
<td>-1.54/-1.17</td>
<td>-1.52/-1.12</td>
</tr>
<tr>
<td>Output Reflection Coefficient</td>
<td>-23.0/-12.85</td>
<td>-23.0/-13.13</td>
<td>-23.0/-12.85</td>
<td>-23.0/-13.13</td>
</tr>
</tbody>
</table>

Voltage Supply = 2.25VDC, CMOS Supply = 1.5VDC
**Table 0.6:** LNA1 input ports comparison in relation to each other

<table>
<thead>
<tr>
<th>Simulation @ 19.3GHz (dB)</th>
<th>Input 1 (on), Input 2 (off)</th>
<th>Input 2 (on), Input1 (off)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Isolation Input1 to Input2</td>
<td>38.56/39.34</td>
<td>75.4/74.49</td>
</tr>
<tr>
<td>Isolation Input2 to Input1</td>
<td>80.71/79.17</td>
<td>37.38/38.3</td>
</tr>
</tbody>
</table>

Voltage Supply = 2.25VDC, CMOS Supply = 1.5VDC

**Table 0.7:** LNA2 input ports comparison in relation to the output

<table>
<thead>
<tr>
<th>Simulation @ 19GHz (dB)</th>
<th>Input 1 (on)</th>
<th>Input 2 (on)</th>
<th>Input 1 (off)</th>
<th>Input 2 (off)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (Input to Output)</td>
<td>15.7</td>
<td>15.7</td>
<td>-36.18</td>
<td>-36.18</td>
</tr>
<tr>
<td>NF</td>
<td>2.83</td>
<td>2.81</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>Isolation (Output to Input)</td>
<td>45.42</td>
<td>45.42</td>
<td>68.76</td>
<td>67.12</td>
</tr>
<tr>
<td>Input Reflection Coefficient</td>
<td>-12.0</td>
<td>-12.0</td>
<td>-1.04</td>
<td>-1.04</td>
</tr>
<tr>
<td>Output Reflection Coefficient</td>
<td>-16.2</td>
<td>-16.2</td>
<td>-16.2</td>
<td>-16.2</td>
</tr>
</tbody>
</table>

Voltage Supply = 2.25VDC, CMOS Supply = 1.5VDC

**Table 0.8:** LNA2 input ports comparison in relation to each other

<table>
<thead>
<tr>
<th>Simulation @ 19.3GHz (dB)</th>
<th>Input 1 (on), Input 2 (off)</th>
<th>Input 2 (on), Input1 (off)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Isolation Input1 to Input2</td>
<td>38.6</td>
<td>53.7</td>
</tr>
<tr>
<td>Isolation Input2 to Input1</td>
<td>53.8</td>
<td>38.4</td>
</tr>
</tbody>
</table>

Voltage Supply = 2.25VDC, CMOS Supply = 1.5VDC

### 3.5.5 LNA1 and LNA2 Transient Analysis and Nonlinearity

Simulations were done to analyze the circuit’s transient response when switching between Input#1 and Input#2 to ensure the required switching times of better than 5us is met. The deciding factor in switching speed is the collector current of Q2 and Q3 governed by the FETs Q2b and Q3b respectfully. The switching rate of “VC” between 0 volts and 1.5 volts was varied on “VC” until the limit of the response of the collector currents was reached as shown in Figure 3.35. The collector current for both transistors respond equally; capable of turning on within 40ns and turning off within 5ns. The turn on time is longer do to the long RC time constant between the ‘turning on’ FET and the base of the ‘turning on’ HBT. The “shorting” input fets Qin1 and Qin2 helps discharging
the base current to decrease shut down time. 40ns limits the switching times to a frequency of 12.5MHz; 125 times the required frequency for this application. However, there is a 55ns delay between the times “VC” changes states to the time the “turn on” transistor response to it and another 15ns for the transistor to reach its 10% turn on current. This 55ns delay can be taken into account by smart programming of the control logic.

Another consideration for switching is making sure no voltage or current spikes occurs causing junction breakdown. The evaluation of Q1 indicates that the collector to emitter voltage will not exceed 0.88 volts. Evaluating Q2 and Q3 indicates that their collector to emitter voltage will not exceed 1.51volts. The latter result is the maximum threshold for VCE as was given in table 3.2. However, there is a discrepancy between the transient analysis and steady state. Steady state analysis indicates 1.10 volts for Q1 VCE and 1.15 volts for Q2 and Q3 VCE.

The transient analysis for LNA2 is near identical to those shown for LNA1 so no further discussion is necessary.

Figure 0.35: LNA1, Control Voltage ‘VC’ vs. Collector Current of Q2 and Q3.
Compressing the expected signal power of -80dBm is highly unlikely but compression analysis was done to make certain the input 1dB compression point (P1dBin) was greater than -40dBm. Figure 3.36 plots P1dBin for Input#1 for LNA1. This plot shows the schematic simulation is 9.54dB higher than that of the simulation using the “rlck” extraction. Still, a P1dBin of -21.16dBm is acceptable. The “rlck” simulation for Input#2 indicates -23.07dBm for P1dBin. This is difference will not have an effect on the expected signal powers.

The simulations for LNA2 two inputs have an expected input 1dB compression point for this layout to be -13.97dBm for Input1 and -13.99dBm for Input2. These graphs can be found in Appendix D. The two inputs’s input 1dB compression points are more identical for this layout than LNA1 because the inputs near identical matching.

Figure 0.36: LNA1, Input#1 P1dB input compression point
CHAPTER 4

RESULTS

Two wafers were received for testing. One wafer was found to be defective with all the die I/O pads shorted together. The entire die on the other wafer proved to work. The ‘KERF'\(^2\) data for this wafer indicated all specified parameters are within limits except beta. Beta is expected to be 600 but this wafer has a beta of 287. It is expected this will lower the gain by 2.4dB. The noise figure should not be greatly affected if the DC current through each transistor is reduced from 4.5mA to 2.6mA, as this will move them to their optimized noise figure current. The test equipment available to test this wafer and the measurement setups along with calibration are discussed in Appendix E.

4.1 LNA1 Measurements

4.1.1 DC Measurements

The first test was connecting the power and control supplies. Setting VCC to 2.25V, CMOS to 1.5V and VC to 0V drew 7.02mA VCC current. Setting VC to 1.5V changed the VCC current to 7.98mA. Several layouts were tested with similar results. The CMOS current draw measured was 46nA when VC = 0V and 7.9nA when VC = 1.5V. All current measurements are 78% of the designed value, as expected due to the low beta of the transistors. The currents could easily be made to match by adjusting the CMOS voltage and or VC voltage. E.g. setting CMOS to 1.57V and VC to 1.52V drew the same 8.85mA of VCC current in both switching states. It was found this slightly

---

\(^2\) KERF is the process of placing test sites of different components throughout the wafer so DC testing can be done to characterize the quality of them. This includes metal lines, mim capacitors, and FETS and HBT transistors.
improved the symmetry performance of the two inputs. These latter voltages were used to bias the chip.

4.1.2 Stability

The next test was stability. The LNA inputs were connected to the network analyzer for the source and the output was connected to the spectrum analyzer for a wide sweep. No oscillations were seen. A second verification of stability was measuring the s-parameters of the device and check S11 and S22. It will be shown next that these measurements remained < 0dB.

The next test was measuring the s-parameters of the device at ambient temperature (22°C) using the 4-port network analyzer. Measurement was done for when Input#1 was on and again when Input#2 was on. Having the 4-port network analyzer allowed capturing all three ports simultaneously. The data was imported into the Agilent’s ADS tool so graphs could be made for easy comparison between the two inputs when at the same state.

4.1.3 S-Parameters

The first comparison is the LNA1 gain as shown in figure 4.1. S(3,1) is the gain for Input#1, when active, to the output and S(7,6) is the gain for Input#2 to the output when active. It shows both inputs peak at the frequency 18GHz, which is close to the 18.25GHz simulated without the matching wirebonds. The difference of 0.6dB in gain is also in good agreement with the simulation but the magnitude is 5.6dB lower than the expected 18dB-2.4dB (beta adjustment) = 15.6dB. It will be shown in Chapter 5 that the differences between the two input gains and their magnitude can be captured using the
proper extraction technique and the reason is related to the inductors used for the matching of the input ports.

The difference in input matching is evident in the measured input return loss for LNA1 shown in figure 4.2. S(1,1) is Input#1 when active, S(2,2) is Input#2 when inactive, S(5,5) is Input#1 when inactive and S(6,6) is Input#2 when active. Comparing the two inputs return losses when inactive show they are equal at -1.5dB, which matches the simulation data. However the return loss when active shows both inputs match moved from the expected 16.4GHz to 19.47GHz for Input#1 and 18.55GHz for Input#2. The magnitude of the measured return loss of 20dB is close to the simulation.

The output return loss measurement graphed in figure 4.3 shows the output match when switching from Input#1 to Input#2. S(3,3) is the output return loss when Input#1 is active and S(7,7) is the output when Input#2 is active. It changes by 0.2dB centered at 18.10GHz which is comparable to the 18.5GHz simulation result, but the magnitude of -7dB is 6dB worse than predicted.

The measured isolation between the output and the active input is graphed in figure 4.4. The isolation of 34dB is about 10dB less then the predicted results.

![Input1 vs. Input2 Gain Comparison](image)

**Figure 0.1:** LNA1 gain comparison between Input#1 when active and Input#2 when active.
**Figure 0.2:** LNA1 input return loss comparison between *Input#1* and *Input#2* in both states.

**Figure 0.3:** LNA1 output return loss comparison between *Input#1* and *Input#2* in both states.
Figure 0.4: LNA1 gain comparison from the output to the active input.

Figure 4.5 consists of four graphs to compare isolation between the output and active input to the isolation between the output and inactive input. The top left graph shows that the isolation from the inactive input to the output is better than 40dB. This is 10dB better than expected and could be in part due to the low gain and higher line resistance. The bottom left graph is the reverse gain from the output to the inactive input. Here the worse case isolation is 34dB for Input#1. The top right graph compares the gain from the active input to the inactive input. The worse case isolation is 27dB from Input#1 to Input#2. The lower right graph compares the gain from the inactive input to the active input. Here the isolation is approximately 46dB for both inputs.
Figure 0.5: LNA1 gain (isolation) between the output and active input to the inactive input.

4.1.4 Noise Figure

The noise figure measurement was done using the setup described in Appendix E. The noise figure and gain for LNA1 measured at ambient temperature is shown in figure 4.6. The noise figure for Input#2 measured at 5.2dB, which is 2.4dB higher than the simulation. The noise figure meter gain measurement agrees well with the measured s-parameter gain. The discrepancy in noise figure is expected to be in part due to the shift in input match and higher than expected transmission line resistance. Input#1 measured 0.2dB higher at 5.4dB. This can attributed in part to the difference in input matching.
The next measurement test was performance variation with temperature. The wafer chuck was programmed to change in temperature from 0°C to 80°C in 10°C increments. The probes had to be adjusted several times throughout this test to compensate for the physical change of the wafer and probes. Water started to condense near 0°C so that became the lower limit of the temperature range.

Figure 4.7 plots the noise figure for both inputs versus temperature change from 0°C to 80°C. It shows the noise figure increases with temperature as expected. Input#1 is higher than Input#2 as expected from the ambient temperature measurement. The rate of increase is 0.11dB/°C for Input1 and 0.12dB/°C for Input2. The gain variation with respect to temperature is shown in figure 4.8. Both inputs decreased in gain with increase in temperature with Input#1 decreasing at a rate of 0.002dB/°C and Input#2 decreased at

Figure 0.6: Noise Figure for Input#2 of LNA1 at 20°C temperature.
a rate of 0.001dB/°C. The input match for the active inputs and the output match did not shift in resonance, but the magnitude of the return loss did decrease by 5dB from 0°C to 80°C for both inputs equally. The output return loss magnitude remained within 0.5dB. It was noted that the input return loss for the inactive Input#1 changed from -2.76dB at 0°C to -1.4dB at 80°C with the majority of change from 0°C to 30°C. Input#2 return loss remained more constant to within +/-0.15dB at -1.3dB. It is expected that condensation was affecting VC because this discrepancy was not seen on other measurements done at ambient temperature.

The last s-parameter test was varying the VCC voltage from 2.23VDC to 2.27VDC in 0.01V increments. It was noted that the VCC current increases 100uA/0.01VDC. No change in input and output match, noise figure and gain was measured.

![NF vs. Temperature](image)

**Figure 0.7:** LNA1 Noise Figure versus Temperature
4.1.5 Transient and Non-Linearity Measurements

No real time oscilloscope was available to measure 19GHz to see how long it took for a port to become active so the oscilloscope was used to measure the transient times of the supply current using a sense resistor. The control line ‘VC’ was used as the trigger. Monitoring the voltage of the sense resistor showed a stabilization time of 48ns, which equates to 10.4MHz. This exceeds the 5us requirement by a factor of 100.

The input 1dB compression point was measured by the method described in Appendix E. Graphing the two inputs together in figure 4.9 shows the compression curve. \textit{Input}#1 compress at -13.64dBm and \textit{Input}#2 compresses at -14.68dBm. These results are closer to the schematic simulated 1dB compression point of approximately -10dBm than the RLCK extracted data point of -20dBm. In either case it is more than required for the application.
**Figure 0.9:** LNA1 Input 1dB Compression Point for Input#1 and Input#2.

### 4.1.6 LNA1 Measurement Summary

Table 4.1 and 4.2 summarizes the s-parameter measurements results. Table 4.3 summarizes the 1dB compression point, the switching times and gain and noise figure variation versus temperature. Overall, the results show a lower gain, higher noise figure and shifts in return loss of the ports when compared to the simulated data. It is expected this is do to the extraction method used for the transmission lines and the inductor model *rfline*. Chapter 5 makes the argument for this.

**Table 0.1:** LNA1 input ports measurement comparison in relation to the output

<table>
<thead>
<tr>
<th>Measurement (dB)</th>
<th>Input 1 (on)</th>
<th>Input 2 (on)</th>
<th>Input 1 (off)</th>
<th>Input 2 (off)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (Input to Output) at 18.00GHz</td>
<td>10.43</td>
<td>9.833</td>
<td>&lt;-42</td>
<td>&lt;-37</td>
</tr>
<tr>
<td>NF at 19GHz</td>
<td>5.47</td>
<td>5.2</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>Isolation (Output to Input) at 18.25GHz</td>
<td>&gt;32</td>
<td>&gt;33</td>
<td>&gt;34</td>
<td>&gt;38</td>
</tr>
<tr>
<td>Input Reflection Coefficient</td>
<td>-19.47 at 19.5GHz</td>
<td>-21.96 at 18.55GHz</td>
<td>-1.5</td>
<td>-1.5</td>
</tr>
<tr>
<td>Output Reflection Coeffic. at 18.1GHz</td>
<td>-7.04</td>
<td>-7.22</td>
<td>-7.22</td>
<td>-7.04</td>
</tr>
</tbody>
</table>
Table 0.2: LNA1 input ports comparison in relation to each other

<table>
<thead>
<tr>
<th>Measurement @ 19.3GHz (dB)</th>
<th>Input 1 (on), Input 2 (off)</th>
<th>Input 2 (on), Input1 (off)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Isolation Input1 to Input2</td>
<td>29</td>
<td>47</td>
</tr>
<tr>
<td>Isolation Input2 to Input1</td>
<td>49</td>
<td>31</td>
</tr>
</tbody>
</table>

Table 0.3: LNA1 Linearity, Switching and Temperature Variations

<table>
<thead>
<tr>
<th>Test Measurement</th>
<th>Input 1</th>
<th>Input 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input P1dB (dBm)</td>
<td>-13.64</td>
<td>-14.68</td>
</tr>
<tr>
<td>Switching Times</td>
<td>48ns</td>
<td>48ns</td>
</tr>
<tr>
<td>Gain Temperature Coefficient (dB/°C)</td>
<td>-0.002</td>
<td>-0.001</td>
</tr>
<tr>
<td>NF Temperature Coefficient (dB/°C)</td>
<td>0.109</td>
<td>0.119</td>
</tr>
</tbody>
</table>

4.2 LNA2 Measurements

The same tests were done for this layout as those that were done for LNA1 with the exception of the temperature variation tests. Details of the test setup can be found in Appendix E and chapter section 4.1.

4.2.1 DC Measurements

Supplying 2.25VDC for VCC, 1.5VDC for CMOS and 0VDC for VC drew 6.65mA of current. Switching states by setting VC to 1.5VDC drew 7.01mA of VCC supply current. The two states could be made equal to 8.85mA by adjusting CMOS to 1.66V and VC to 1.62V. These latter values were used for the remaining measurements.

4.2.2 Stability

This layout proved to be stable by using the spectrum analyzer like that what was done for LNA1. The same second verification of stability was done by measuring the s-parameters of the device and check S11 and S22. This layout also meets the stability requirement of S11 and S22 < 0dB.
4.2.3 S-Parameters

The s-parameter measurements were taken and are plotted in a similar setup as that was done for LNA1. Figure 4.10 shows the gain for the inputs when active. The graph indicates that Input#1 has a peak gain of 10dB at 16.9GHz (S2,1) and Input#2 has a peak gain at 9.4dB at 16.6GHz (S7,6). This gain is closer to the expected simulated gain of 13.5dB (taking beta into account), than that for LNA1. Measuring other LNA2 die on the wafer showed consistent gain with variations within +/-0.3dB. Input#1 gain was always greater than Input#2, which wasn’t expected as the simulation results showing the two gains identical to each other. Like for LNA1, Chapter 5 will show that using the proper extraction setup will capture the differences between the two input gains and their magnitudes, which is related the inductor used for the input matching like that in LNA1.

The input return loss is graphed in figure 4.11. It shows that the matching shifted up in frequency like LNA1, but not as far. The magnitude decrease slightly compared to the simulation. Another unexpected result is the difference in matching between Input#1 (S1,1) and Input#2 (S6,6); they are equal in the simulation. The two inputs are equal in magnitude when they are off.

The output return loss graphed in figure 4.12 is a larger surprise having a 5dB discrepancy when Input#1 is active (S3,3) to when Input#2 is active (S7,7). Again, the simulation did not capture this. The test setup was checked and several LNA2 layouts were tested to validate this result. The best match occurs at 15GHz, which is 4.3GHz lower than that simulated in chapter 3.
Figure 4.13 is a graph showing the reverse gain from the output port to the active input. The isolation for Input#1 (S1,3) is 25dB less than for Input#2 (S6,7). It is expected that this is because of the poorer output matching for when Input#1 is active.

**Figure 0.10:** LNA2 gain comparison between the Input#1 when active and Input#2 when active.

**Figure 0.11:** LNA2 input return loss comparison between Input#1 and Input#2 in both states.
**Figure 0.12:** LNA2 output return loss comparison between Input#1 and Input#2 in both states.

**Figure 0.13:** LNA2 gain comparison from the output to the active input.

Figure 4.14 consists of four graphs comparing the isolation between the inactive input to the output and active input like those done for LNA1 in figure 4.5. The isolation for this layout is more symmetrical when compared to LNA1. LNA2 does have about 8dB higher isolation from the output to the inactive inputs when compared to LNA1 (bottom left graph). This could be due to a longer distance between the ports.
4.2.4 Noise Figure

Noise figure measurements showed that Input#1 averaged 5.1dB and Input#2 averaged 5.2dB. This is 2.3dB higher than expected similar to LNA1. A screen capture of the noise figure meter is provided in figure 4.15. LNA2 noise figure averaged 0.2dB less than that for LNA1. These deltas are consistent with the deltas in the simulation.

Figure 0.14: LNA2 gain (isolation) between the output and active input to the inactive input.
Figure 0.15: Noise Figure for Input#1 of LNA2 at 20°C temperature.

4.2.5 Transient and Non-Linearity Measurements

The switching times were measured like those for LNA1. It was found that the switching times of 48ns for this layout are identical to LNA1. The input 1dB compression point was measured to be -13.04dBm for Input#1 and -13.84dBm for Input#2. The two inputs in this layout are in more of agreement than for LNA1.

4.2.6 LNA2 Measurement Summary

Table 4.4 and 4.5 summarizes the s-parameter measurements results. Table 4.6 summarizes the 1dB compression point and the switching times. Like LNA1, the results show a lower gain, higher noise figure and shifts in return loss of the ports when compared to the simulated data.
### Table 0.4: LNA2 input ports measurement comparison in relation to the output

Supply: VCC = 2.25V @ 8.8mA, CMOS =1.57V, VC = 0/1.52V

<table>
<thead>
<tr>
<th>Measurement (dB)</th>
<th>Input 1 (on)</th>
<th>Input 2 (on)</th>
<th>Input 1 (off)</th>
<th>Input 2 (off)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (Input to Output) at 16.60GHz</td>
<td>10.0</td>
<td>9.4</td>
<td>&lt;-32</td>
<td>&lt;-34</td>
</tr>
<tr>
<td>NF at 19GHz</td>
<td>5.10</td>
<td>5.18</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>Isolation (Output to Input) at 18.00GHz</td>
<td>&gt;34</td>
<td>&gt;47</td>
<td>&gt;45</td>
<td>&gt;47</td>
</tr>
<tr>
<td>Input Reflection Coefficient</td>
<td>-12.75 at 18.79GHz</td>
<td>-14.45 at 18.35GHz</td>
<td>-1.84</td>
<td>-1.92</td>
</tr>
<tr>
<td>Output Reflection Coeff. at 15.0GHz</td>
<td>-11.18</td>
<td>-16.0</td>
<td>-16.0</td>
<td>-11.18</td>
</tr>
</tbody>
</table>

### Table 0.5: LNA2 input ports comparison in relation to each other

<table>
<thead>
<tr>
<th>Measurement @ 19.3GHz (dB)</th>
<th>Input 1 (on), Input 2 (off)</th>
<th>Input 2 (on), Input 1 (off)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Isolation Input1 to Input2</td>
<td>35</td>
<td>45</td>
</tr>
<tr>
<td>Isolation Input2 to Input1</td>
<td>45</td>
<td>35</td>
</tr>
</tbody>
</table>

### Table 0.6: LNA1 Linearity and Switching Times

<table>
<thead>
<tr>
<th>Test Measurement</th>
<th>Input 1</th>
<th>Input 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input P1dB (dBm)</td>
<td>-13.04</td>
<td>-13.84</td>
</tr>
<tr>
<td>Switching Times</td>
<td>48ns</td>
<td>48ns</td>
</tr>
</tbody>
</table>
CHAPTER 5

EXTRCTIONS AND MODELS REVISITED

In this chapter the measurements presented in Chapter 4 will be compared to the simulations in Chapter 3 and in the appendices. The various causes of discrepancy will be discussed. It will be shown that there are three primary factors causing the differences besides the low Beta. One factor is the extraction deck and design models used for the initial design had to be improved; specifically the model singlewire used in LNA1. The second factor is due the way the extraction tool was setup, which had its most effect on the transmission lines by over simplifying the mutual and self inductance extractions and not taking the skin effect loss into account (See Appendix A). The third factor is the model for the matching inductors does not adequately capture the current returns for a given layout.

Table 5.1 summarizes the measured versus the model results for gain, NF and input and output match for both designs. The data for both layouts show that the gain was considerably lower and the noise figure higher than the simulated data. It also shows that both matching inputs for the two designs shifted up in frequency and the output match shifted down.
Table 0.1: Simulation versus measured data (Design Kit V1.0.3.1HP)

<table>
<thead>
<tr>
<th></th>
<th>LNA1</th>
<th>LNA2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Peak Gain</td>
<td>Lowest NF</td>
</tr>
<tr>
<td>Simulated Input1</td>
<td><a href="mailto:17.9dB@18.25GHz">17.9dB@18.25GHz</a></td>
<td><a href="mailto:2.8dB@17.5GHz">2.8dB@17.5GHz</a></td>
</tr>
<tr>
<td>Measured Input1 Data</td>
<td>10.43dB@18GHz</td>
<td><a href="mailto:5dB@19.56GHz">5dB@19.56GHz</a></td>
</tr>
<tr>
<td>Simulated Input2</td>
<td><a href="mailto:18.25dB@18.25GHz">18.25dB@18.25GHz</a></td>
<td><a href="mailto:2.7dB@17.5GHz">2.7dB@17.5GHz</a></td>
</tr>
<tr>
<td>Measured Input2 Data</td>
<td>9.83dB@18GHz</td>
<td><a href="mailto:5.4dB@19.56GHz">5.4dB@19.56GHz</a></td>
</tr>
</tbody>
</table>

5.1 Beta and Design Kit Adjustment

It was mentioned in Chapter 4 that the DC beta for this wafer is 287 instead of the nominal 600. The process measured beta was applied to the original models and simulated again using the same extraction method described in Chapter 3. The results of this are compared in table 5.2 for only Input1 of LNA1 for simplicity. Input2 and the inputs for LNA2 had similar trends. The table shows that the primary changes were the gain decreased by 2.3dB and the noise figure increased by 0.2dB. This still does account for the discrepancies in the measurements.

Table 0.2: Simulation results for before and after beta adjustment for LNA1

<table>
<thead>
<tr>
<th></th>
<th>LNA1</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Peak Gain</td>
<td>Lowest NF</td>
</tr>
<tr>
<td>V1.0.3.0HP Input1</td>
<td><a href="mailto:17.9dB@18.25GHz">17.9dB@18.25GHz</a></td>
<td><a href="mailto:2.8dB@17.5GHz">2.8dB@17.5GHz</a></td>
</tr>
<tr>
<td>Beta Adjustment</td>
<td><a href="mailto:15.6dB@18.25GHz">15.6dB@18.25GHz</a></td>
<td><a href="mailto:3.2dB@17.5GHz">3.2dB@17.5GHz</a></td>
</tr>
</tbody>
</table>

Another change to occur between the original design and process were two more design kit releases. The modeling group took data from other test-site runs to improve
the models after this design was released to fabrication. Simulations like that in Chapter 3 were repeated using the latest design kits including the adjusted beta. The effect that these updated design kits has on the simulation results are shown in table 5.3. Only Input1 of LNA1 is shown for simplicity. The actual measurement is included in the last line of the table for easy comparison. The reason for the dramatic change between design kit V1.0.6.1HP to V1.1.0.0HP will be shown to be attributed to the improvement of the transmission line model singlewire working with the extraction tool. LNA2 had minor changes with respect to design kits using the default ‘RLCK’ extraction because it does not use the transmission line model singlewire in its layout. The latest design kit results for LNA1 are the closest to the measured data, but there are still significant differences.

**Table 0.3: Simulation result comparison between design kits including the beta adjustment for LNA1**

<table>
<thead>
<tr>
<th>LNA1 Beta Adjusted</th>
<th>Peak Gain</th>
<th>Lowest NF</th>
<th>Best Input Match (On)</th>
<th>Best Output Match</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1.0.3.0HP Input1</td>
<td><a href="mailto:15.6dB@18.25GHz">15.6dB@18.25GHz</a></td>
<td><a href="mailto:3.2dB@17.5GHz">3.2dB@17.5GHz</a></td>
<td><a href="mailto:-23dB@15.8GHz">-23dB@15.8GHz</a></td>
<td><a href="mailto:-14.2dB@18.4GHz">-14.2dB@18.4GHz</a></td>
</tr>
<tr>
<td>V1.0.6.1HP Input1</td>
<td><a href="mailto:15.4dB@18.25GHz">15.4dB@18.25GHz</a></td>
<td><a href="mailto:3.2dB@17.3GHz">3.2dB@17.3GHz</a></td>
<td><a href="mailto:-22.7dB@15.8GHz">-22.7dB@15.8GHz</a></td>
<td><a href="mailto:-14.0dB@18.58GHz">-14.0dB@18.58GHz</a></td>
</tr>
<tr>
<td>V1.1.0.0HP Input1</td>
<td><a href="mailto:12.8dB@19.2GHz">12.8dB@19.2GHz</a></td>
<td><a href="mailto:4.2dB@15.8GHz">4.2dB@15.8GHz</a></td>
<td><a href="mailto:-30.3dB@15.4GHz">-30.3dB@15.4GHz</a></td>
<td><a href="mailto:-13.8dB@19.7GHz">-13.8dB@19.7GHz</a></td>
</tr>
<tr>
<td>Measured Input1 Data</td>
<td>10.43dB@18GHz</td>
<td><a href="mailto:5dB@19.56GHz">5dB@19.56GHz</a></td>
<td><a href="mailto:-19.47dB@19.5GHz">-19.47dB@19.5GHz</a></td>
<td><a href="mailto:-7.05dB@18.1GHz">-7.05dB@18.1GHz</a></td>
</tr>
</tbody>
</table>

The HBT model was considered, but adjusting the parameters that would cause the gain to decrease and noise figure to increase showed that the input return loss would decrease in magnitude and not increase in frequency. The lead modeler for the transistor [16] insisted that the model’s frequency performance is guaranteed to be tied to its DC beta\(^3\). Besides beta, the remaining parameters for the transistor such as junction capacitances and base, collector and emitter resistance were well within bounds so beta

---

\(^3\) It is suggested that for future designs that space is made on the wafer to place a transistor of the same size used in the design with AC probe pads to allow frequency testing.
alone does not adequately explain the discrepancies between the simulated and measured data. It was found from conversations with the Assura design team [18] and the kit design team [19] that improvements were made to the extraction deck and the transmission line model *singlewire*, which will be noticed when using the extraction tool with all the options available to it. Describing these options and changes are best done by using them to reanalyze the designs as discussed in following sections.

5.2 **Input Transmission Line Loss**

The original setup of the extraction tool extracted DC resistance of the wire but not skin effect. In this section we estimate the skin effect will have on the modeling. The total line length for each input of LNA1 is 886um and the total line length for LNA2 is 1.75mm for *Input1* and 1.68mm for *Input2*. This is the main difference between LNA1 and LNA2.

Assuming that the transmission line loss is dominated by the conductor and not the substrate, the loss for a microstrip can be approximated using equations 5.1 and 5.2 [17].

\[
\alpha_c = \frac{R_s}{(Z_0 \cdot W)} \text{ (Np/m)} \quad (5.1)
\]

\[
R_s = \sqrt{\frac{\omega \cdot \mu_0}{(2 \cdot \sigma)}} \quad (5.2)
\]

Where \(\alpha_c\) is the attenuation constant of the conductor and \(R_s\) is the surface resistance of the metal which the signal propagates including the skin effect. The metal for these transmission lines is aluminum, which has a conductivity of \(\sigma = 3.816 \times 10^7\) S/m, so the surface resistance is 0.0443 \(\Omega\). The transmission line width is \(W=10\)um and the characteristic impedance is \(Z_0 = 50\) \(\Omega\). Substituting these parameters into equation 5.1 equates to an attenuation constant of 88.671Np/m or 770.55dB/m. 770.6dB/m means
that the expected added loss due to skin effect will be 0.683dB for LNA1 and 1.349dB for Input#1 of LNA2 and 1.297dB for Input#2 of LNA2. The skin effect is large enough to require consideration and the difference between the two designs correlates with the measurement difference of 0.5dB, but this does not explain the large discrepancy between the measured data presented in chapter 4 and the simulated data presented in chapter 3. The measured gain of LNA2 is closer to that simulated for LNA2 than the measured gain of LNA1 is to that simulated for LNA1.

5.2.1 Improved Transmission Line Extraction

LNA2 was the first design analyzed because its extraction data is closer to the measurements and therefore thought to be more accurate. Phone conversations took place with the leading support member of the Cadence Assura design team to discuss the results [18]. It was found that the extracted RLCK options ‘PEEC,’ ‘LADDER’ and substrate extraction (as discussed in Appendix A) should be used together at these frequencies. Computers capable of simulating large areas of the layout (See figure A.2) with these three options engaged simultaneously became available since the original simulations that were done in Chapter 3. However, the computer still had issues extracting areas larger than shown in figure A.2 due to memory limitations.

These options were applied to the latest design kit V1.1.0.0HP with the appropriate beta and re-simulated. The effect this had on the gain, noise figure and matching can be compared in table 5.4. The simulation results using the using the loop method for inductance is given as ‘V1.1.0.0HP’. This method captures gain and matching differences between the two inputs. Adding the PEEC and LADDER options for extractions produces simulation results given as ‘PEEC+LADDER Option’ in the
same table. Using the ‘PEEC+LADDER’ option could only be performed on 80% of the transmission lines due to computer limitations, so the areas not extracted had the parasitic elements added manually. These elements were determined by opening the netlist generated from the extraction tool and analyzing the values were given for the extracted portion of the transmission lines. Table 5.4 shows that extracting ground inductance and the skin effect decreased the gain by more than 3dB and increase the noise figure by 1.3dB for Input1 and 1.9dB for Input2. The input and output return loss also better correlates with the measured data. However, there are still differences between the simulated results and measured data, particularly the frequency, which results from discrepancies between the modeled inductance and actual inductance of the inductors used for matching. This is explained next.

Table 5.4: Comparing ‘RLCK’ to ‘PEEC+LADDER’ extraction simulations for LNA2

<table>
<thead>
<tr>
<th>LNA2 Beta Adjusted</th>
<th>Peak Gain</th>
<th>Lowest NF</th>
<th>Best Input Match</th>
<th>Best Output Match</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1.1.0.0HP Simulated (Input1 active)</td>
<td><a href="mailto:13.6dB@17.3GHz">13.6dB@17.3GHz</a></td>
<td><a href="mailto:3.3dB@16.6GHz">3.3dB@16.6GHz</a></td>
<td><a href="mailto:-20.2dB@15.7GHz">-20.2dB@15.7GHz</a></td>
<td><a href="mailto:-12.0dB@17.9GHz">-12.0dB@17.9GHz</a></td>
</tr>
<tr>
<td>PEEC+LADDER Options (Input1 active)</td>
<td><a href="mailto:11.0dB@16.3GHz">11.0dB@16.3GHz</a></td>
<td><a href="mailto:4.6dB@17.1GHz">4.6dB@17.1GHz</a></td>
<td><a href="mailto:-12.2dB@16.1GHz">-12.2dB@16.1GHz</a></td>
<td><a href="mailto:-14.9dB@16.2GHz">-14.9dB@16.2GHz</a></td>
</tr>
<tr>
<td>Measured Input1 Data</td>
<td><a href="mailto:10.0dB@16.9GHz">10.0dB@16.9GHz</a></td>
<td>5.1dB@19GHz</td>
<td><a href="mailto:-12.75@18.7GHz">-12.75@18.7GHz</a></td>
<td>-11.18dB@15GHz</td>
</tr>
<tr>
<td>V1.1.0.0HP Simulated (Input2 active)</td>
<td><a href="mailto:15.0dB@16.45GHz">15.0dB@16.45GHz</a></td>
<td><a href="mailto:3.0dB@16.5GHz">3.0dB@16.5GHz</a></td>
<td><a href="mailto:-10.7dB@14.2GHz">-10.7dB@14.2GHz</a></td>
<td><a href="mailto:-12.7dB@17.9GHz">-12.7dB@17.9GHz</a></td>
</tr>
<tr>
<td>PEEC+LADDER Options (Input2 active)</td>
<td><a href="mailto:11.5dB@16.3GHz">11.5dB@16.3GHz</a></td>
<td><a href="mailto:4.7dB@17.4GHz">4.7dB@17.4GHz</a></td>
<td><a href="mailto:-13.5dB@16.15GHz">-13.5dB@16.15GHz</a></td>
<td><a href="mailto:-16.8dB@16.2GHz">-16.8dB@16.2GHz</a></td>
</tr>
<tr>
<td>Measured Input2 Data</td>
<td><a href="mailto:9.4dB@16.6GHz">9.4dB@16.6GHz</a></td>
<td>5.2dB@19GHz</td>
<td><a href="mailto:-14.45dB@18.35GHz">-14.45dB@18.35GHz</a></td>
<td><a href="mailto:-16.1dB@14.94GHz">-16.1dB@14.94GHz</a></td>
</tr>
</tbody>
</table>

5.2.2 Matching Inductors Analyzed

The Smith chart in figure 5.1 shows the measured input/output reflection coefficients and provides the best representation of what is going on with the input/output matching. There is an obvious mismatch between the two input ports. The last extraction captures this mismatch because of the improved models of the transmission line that couple between the input pads and the matching circuit. But the transmission
line inductors were not improved because the extraction tool ignores them since they have models in the design kit. The question was whether the actual inductance was different from the model. It was thought that this could be proven since all input matching inductors where similar in value and layout. The output matching inductors for both design where also done in similar manner except the inductor in LNA2 had more M1 metal for the current return. By manually adjusting both input matching inductors from 410pH to 315pH for a 23% decrease, and adjusting the matching capacitors from 184.6fF to 188fF for a 1.8% increase resulted in a better input match with the measured data as be seen in table 5.5 under LC Adjustments. This table also shows the result of the output match for when the given input is active after increasing the output matching inductor by 22% from 389pH to 473pH and its matching capacitor increased 7.6% from 198.6fF to 213.7fF. The best simulated output return loss is -12.5dB at 15GHz for when Input1 is active and -16.0dB at 15GHz for when Input2 is active.

Table 0.5: Comparing ‘RLCK’, ‘PEEC+LADDER’ and post LC adjustments for LNA2

<table>
<thead>
<tr>
<th>LNA2 Beta Adjusted</th>
<th>Peak Gain</th>
<th>Lowest NF</th>
<th>Best Input Match</th>
<th>Best Output Match</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1.1.0.0HP Simulated (Input1 active)</td>
<td><a href="mailto:13.6dB@17.3GHz">13.6dB@17.3GHz</a></td>
<td><a href="mailto:3.3dB@16.6GHz">3.3dB@16.6GHz</a></td>
<td><a href="mailto:-20.2dB@15.7GHz">-20.2dB@15.7GHz</a></td>
<td><a href="mailto:-12.0dB@17.9GHz">-12.0dB@17.9GHz</a></td>
</tr>
<tr>
<td>PEEC+LADDER Options (Input1 active)</td>
<td><a href="mailto:11.0dB@16.3GHz">11.0dB@16.3GHz</a></td>
<td><a href="mailto:4.6dB@17.1GHz">4.6dB@17.1GHz</a></td>
<td><a href="mailto:-12.2dB@16.1GHz">-12.2dB@16.1GHz</a></td>
<td><a href="mailto:-14.9dB@16.2GHz">-14.9dB@16.2GHz</a></td>
</tr>
<tr>
<td>LC Adjustment (Input1 active)</td>
<td><a href="mailto:10.5dB@16.9GHz">10.5dB@16.9GHz</a></td>
<td><a href="mailto:4.8dB@19.1GHz">4.8dB@19.1GHz</a></td>
<td><a href="mailto:-12.2dB@18.7GHz">-12.2dB@18.7GHz</a></td>
<td>-12.5dB@15GHz</td>
</tr>
<tr>
<td>Measured Input1 Data</td>
<td><a href="mailto:10.0dB@16.9GHz">10.0dB@16.9GHz</a></td>
<td>5.1dB@19GHz</td>
<td><a href="mailto:-12.75@18.7GHz">-12.75@18.7GHz</a></td>
<td>-11.18dB@15GHz</td>
</tr>
<tr>
<td>V1.1.0.0HP Simulated (Input2 active)</td>
<td><a href="mailto:15.0dB@16.45GHz">15.0dB@16.45GHz</a></td>
<td><a href="mailto:3.0dB@16.5GHz">3.0dB@16.5GHz</a></td>
<td><a href="mailto:-10.7dB@14.2GHz">-10.7dB@14.2GHz</a></td>
<td><a href="mailto:-12.7dB@17.9GHz">-12.7dB@17.9GHz</a></td>
</tr>
<tr>
<td>PEEC+LADDER Options (Input2 active)</td>
<td><a href="mailto:11.5dB@16.3GHz">11.5dB@16.3GHz</a></td>
<td><a href="mailto:4.7dB@17.4GHz">4.7dB@17.4GHz</a></td>
<td><a href="mailto:-13.5dB@16.15GHz">-13.5dB@16.15GHz</a></td>
<td><a href="mailto:-16.8dB@16.2GHz">-16.8dB@16.2GHz</a></td>
</tr>
<tr>
<td>LC Adjustment (Input2 active)</td>
<td><a href="mailto:10.4dB@16.6GHz">10.4dB@16.6GHz</a></td>
<td><a href="mailto:4.9dB@19.2GHz">4.9dB@19.2GHz</a></td>
<td><a href="mailto:-13.1dB@18.5GHz">-13.1dB@18.5GHz</a></td>
<td>-16.0@15GHz</td>
</tr>
<tr>
<td>Measured Input2 Data</td>
<td><a href="mailto:9.4dB@16.6GHz">9.4dB@16.6GHz</a></td>
<td>5.2dB@19GHz</td>
<td><a href="mailto:-14.45dB@18.35GHz">-14.45dB@18.35GHz</a></td>
<td><a href="mailto:-16.1dB@14.94GHz">-16.1dB@14.94GHz</a></td>
</tr>
</tbody>
</table>

Moving the resonance of the matching circuits for these ports affected the gain by decreasing it as given in the table. The gain for Input1 decreased 0.5dB to 10.5dB and...
shifted up in frequency to 16.9GHz. This gain is within 0.5dB of the measured gain for this port and peaking at the same frequency. The gain for Input#2 decreased 1.1dB to 10.4dB and shifted up in frequency to 16.6GHz. This gain is within 1dB of the measured gain for this port and peaking at the same frequency. The lowest noise figure changed less than 0.2dB in magnitude but did shift up in frequency from 18.5GHz to 19GHz. This is primarily due to the input matching shifting upward in frequency. The 1dB difference between simulated and measured noise figure and the higher simulated gain could be explained by the portion of the transmission lines that were extracted.

The simulated data is not identical to the measured data but it does follow the trend more closely than the simulated results in Chapter 3. It is expected that the matches would be closer to the measured data if full extractions could be done on the transmission lines. These results indicate that the MIM capacitor models are accurate but the inductor models rfline do not appear to capture all the parasitic components. Both input and output matching inductors are DC blocked using five 1pF MIM capacitors in parallel, and we considered the possibility that this contributes to model error. However, the inputs’ matching inductors are ‘shorter’ than modeled and the output matching inductor is ‘longer’ than modeled, so the blocking capacitors are unlikely to be a cause. It will be shown later that the LNA1 simulations require the same adjustments in the inductors.

Plots showing input match and output match are shown in figures 5.2 and 5.3 respectfully. These plots compare extraction results and the results after adjusting the matching inductors for each input when active. The gain plot in figure 5.4 shows the gain for Input2 before and after adjusting the inductors. These plots can be compared to the measured results given in Chapter 4.
Figure 0.1: Smith chart plotting the two measured inputs and output match for LNA2. S(1,1), marked by M8, is the match for Input#1 when active. S(6,6), marked by M10, is the match for Input#2 when active. S(3,3) is the output match, marked by M11, when Input#1 is active and S(7,7) is the output match, marked by M12, when Input#2 is active.

Figure 0.2: LNA2 simulated input return loss for Input#1 and Input#2 when active. ‘S11 dB20_In1 On peec clad sub’ is Input1 after extraction before matching adjustment. ‘S11 dB20_In2 On peec clad sub’ is Input2 after extraction before matching adjustment. ‘S11 dB20_In1 On LC adjusted’ is Input1 after extraction and after matching adjustment. ‘S11 dB20_In2 On LC adjusted’ is Input2 after extraction and after matching adjustment.
Figure 0.3: LNA2 simulated output return loss for Input#1 and Input#2 when active. ‘S22 dB20_In1 On peeclad_sub’ is Input1 after extraction before matching adjustment. ‘S22 dB20_In2 On peeclad_sub’ is Input2 after extraction before matching adjustment. ‘S22 dB20_In1 On LC adjusted’ is Input1 after extraction and after matching adjustment. ‘S22 dB20_In2 On LC adjusted’ is Input2 after extraction and after matching adjustment.

Figure 0.4: LNA2 simulated gain for Input2. ‘S21 dB20_peeclad_sub’ is Input2 gain after extraction but before input and output matching adjustment. ‘S21 dB20_LC adj’ is Input2 gain after extraction and input and output matching adjustment.
5.3 LNA1 Extraction Revisited

Using all the extraction options for the LNA2 layout and adjusting the matching inductors accurately captured noise figure, the matching and the gain to within 1dB. The inductors primarily affected the frequency at which the best return loss occurred. It was expected that most of the simulated matching error for LNA1 would be due to the inductors as well. Simulations using the standard ‘RLCK’ extractions were done using the latest design kit and setting beta to 287. The results are shown in table 5.6 as ‘V1.1.0.0HP’. Repeating the simulations using the added PEEC and LADDER options resulted in those shown as ‘PEEC+LADDER Options’. Having these options engaged reduced the gain 2.0dB. 1.8dB of this reduction was captured by the option PEEC alone, not the skin effect option LADDER because most of the skin effect loss occurred in the singlewire model, which was already included in the first simulation.

<table>
<thead>
<tr>
<th>LNA1 Beta Adjusted</th>
<th>Peak Gain</th>
<th>Lowest NF</th>
<th>Best Input Match</th>
<th>Best Output Match</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1.1.0.0HP Simulated (Input1)</td>
<td><a href="mailto:12.8dB@19.2GHz">12.8dB@19.2GHz</a></td>
<td><a href="mailto:4.2dB@15.8GHz">4.2dB@15.8GHz</a></td>
<td><a href="mailto:-30.3dB@15.4GHz">-30.3dB@15.4GHz</a></td>
<td><a href="mailto:-13.8dB@19.7GHz">-13.8dB@19.7GHz</a></td>
</tr>
<tr>
<td>PEEC+LADDER Options (Input1)</td>
<td><a href="mailto:10.8dB@18.1GHz">10.8dB@18.1GHz</a></td>
<td><a href="mailto:4.4dB@17.3GHz">4.4dB@17.3GHz</a></td>
<td><a href="mailto:-16.9dB@15.8GHz">-16.9dB@15.8GHz</a></td>
<td><a href="mailto:-8.1dB@18.6GHz">-8.1dB@18.6GHz</a></td>
</tr>
<tr>
<td>Measured Input1 Data</td>
<td>10.43dB@18GHz</td>
<td><a href="mailto:5dB@19.56GHz">5dB@19.56GHz</a></td>
<td><a href="mailto:-19.47dB@19.5GHz">-19.47dB@19.5GHz</a></td>
<td><a href="mailto:-7.05dB@18.1GHz">-7.05dB@18.1GHz</a></td>
</tr>
<tr>
<td>V1.1.0.0HP Simulated (Input2)</td>
<td><a href="mailto:13.6@19.2GHz">13.6@19.2GHz</a></td>
<td><a href="mailto:4.2dB@16.6GHz">4.2dB@16.6GHz</a></td>
<td><a href="mailto:-38.5dB@16.0GHz">-38.5dB@16.0GHz</a></td>
<td><a href="mailto:-13.8dB@19.7GHz">-13.8dB@19.7GHz</a></td>
</tr>
<tr>
<td>PEEC+LADDER Options (Input2)</td>
<td><a href="mailto:10.3dB@18.0GHz">10.3dB@18.0GHz</a></td>
<td><a href="mailto:4.4dB@16.8GHz">4.4dB@16.8GHz</a></td>
<td><a href="mailto:-17.8dB@15.9GHz">-17.8dB@15.9GHz</a></td>
<td><a href="mailto:-8.6dB@18.7GHz">-8.6dB@18.7GHz</a></td>
</tr>
<tr>
<td>Measured Input2 Data</td>
<td>9.83dB@18GHz</td>
<td><a href="mailto:5.4dB@19.6GHz">5.4dB@19.6GHz</a></td>
<td><a href="mailto:-21.96dB@18.6GHz">-21.96dB@18.6GHz</a></td>
<td><a href="mailto:-7.22sB@18.1GHz">-7.22sB@18.1GHz</a></td>
</tr>
</tbody>
</table>

The latest design kit improves the singlewire model by including an extraction of the ground returns. Figure 5.5 shows a key point in the layout where this becomes critical for accurate simulations. Each layout component in the design kit has a boundary defining it called a pcell. Current returns from the ends of the inductors via ground metal
that includes “ground returns” 1 and 2. These ground returns connect directly to the ground of the model *singlewire* and cause deviations from the ideal model. The original extraction deck treated the ground contained within the *singlewire* pcell boundary as ideal because of where the boundary was drawn (see figure 5.5). This ideal ground did not cause any discrepancies when using the standard ‘RLCK’ option in Assura because this option treats all ground as ideal. The latest kit shrank the boundary of the pcell so that the outside ground could be extracted properly. The effect this had can be seen when comparing the peak gain using PEEC mode in the original design kit to that of this design kit. The peak gain for *Input1* from the original PEEC extraction shown in figure 3.26 is 16dB. Taking the beta into account reduces this gain to 13.6dB. Using the latest design kit reduces the gain to 10.8dB. Further improvement can be made to the *singlewire* ground to allow PEEC to perform a better extraction by adding ground strips orthogonal to the pcell ground strips, which currents run parallel to the transmission line wire. The ground strips of the pcell can be seen in figure 5.5 as vertical lines (see Chapter 3 for further details).

Improvement was also made to the extraction deck to prevent double counting of parasitic elements. Double counting occurs when the extraction tool calculates parasitic elements twice for overlapping polygons on the same metal layer.

The extraction and model improvements capture a large portion of the gain and noise figure discrepancy when compared to the measured results, but the matching, particularly the input matching, requires further analysis. The input matching discrepancy also affects the frequency of where the minimal noise figure occurs. As was shown for LNA2, the LNA1 discrepancies are related to the inductors used for matching.
**Figure 0.5:** LNA1, Input1 magnified to show the degenerate and matching inductor ground return connections around the common emitter.

### 5.3.1 Matching Inductors Analyzed

Adjusting the matching components for this extraction to match the measured data required adjustments similar to those that were done for LNA2. The Smith chart in figure 5.6 shows the two inputs and output measured impedances. The close symmetry of the two input matches and the output match for both switching states indicate that both transmission paths are nearly identical. This is because the transmission line *singlewire* from Q2 to Q1 and Q3 to Q1 are equal thus having equal phase shift and impedance between two inputs to Q1. The question is whether the adjustment required for the extracted matching circuitry to match the measured data is similar to that which was seen for LNA2.
**Figure 0.6:** Smith chart plotting the two measured inputs and output match for LNA1. S(1,1), marked by M8, is the match for *Input#1* when active and S(5,5) is the match when *Input#1* is inactive, S(6,6), marked by M9, is the match for *Input#2* when active and S(2,2) is the match for *Input#2* when inactive, S(3,3) is the output match when *Input#1* is active and S(7,7) is the output match when *Input#2* is active.

The inductance of the matching inductor for *Input#1* had to be decreased 26.1% to 325pH, and the capacitor had to be increased 8% to 180fF in order for the simulated input return loss to match the measured data. Likewise for *Input#2*, the inductance was decreased 23.2% to 338pH and the capacitance increased 9.1% to 182.2fF. The required change in the inductance is similar to LNA2. This was expected since the inductors’ return paths are similar in that they were placed less than 50um away from the inductor (see figure 5.5). The inductor for *Input#1* required 2.8% more decrease than *Input#2* because of the extra ground paths available to it.

The adjustments required to the output matching components so the simulated output return loss equaled the measured return loss was similar to those that were done for LNA2. The matching inductor had to be increased by 14.1% to 671.8pH and the capacitance increased by 3.1% to 59.0fF. The inductance increase is 25% greater than that required for LNA2 because it was laid out with less low resistive current return path. The capacitance had to be increased 3.1% instead of 8% compared to LNA2. A closer
view of the layout section for the output is shown in figure 5.7. The distance from the inductor to the nearest current return path is 75um meeting the 50um distance requirement. This distance is less than the 95um distance for the output matching inductor in LNA2. The measured results for both layouts indicate that the model underestimated the inductor’s effective length, with LNA2 having greater error than LNA1.

Figure 0.7: LNA1, output magnified to show the matching inductor and MIM capacitors connecting the common base stage to the transmission line leading to the output pads (not shown). The transmission lines connect the two inputs common emitter stage has been removed.

The inductors for both designs caused the largest error in simulation. It was questioned if the excessive ground returns for the input matching inductors leading to their decrease in effective length could be captured by extraction. All matching inductors in the layout had their pcell identity removed so the extraction tool would not associate the metal line to the model rfline. This allowed the extraction tool to extract self and mutual inductances of the line to determine the equivalent inductance. A study of the input and output matching inductor for this design is provided in Appendix A: Assura and Momentum Compared. After extraction, the simulation was redone and the results
tabulated in table 5.7 as ‘Flatten $rfline$ and C Adjustment.’ The capacitors were left at their modified values. Very good correlation exists between this simulation and the measured data with a gain error of 1dB and less than 1dB difference in noise figure. The matching correlation is better for $Input1$ than $Input2$ but the $Input2$ results are still closely matched. The frequency responses of these key simulations are plotted in Figure 5.8, so comparisons can be made between these simulations to the measured results in Chapter 4 and the original extraction results in Chapter 3 and Appendix C. The return loss is not as exact to the measured results when compared to manually adjusting the inductors’ values, but it better represents the inductance of the inductor than the original model $rfline$ (see Appendix A: Assura and Momentum Compared). The effect that the Q of the matching inductors, determined in Appendix A: Assura and Momentum Compared, can be seen in the return loss plots. The output return loss has a much broader match because of its matching inductor Q of 8.1 when compared to the Q of 12 for the inductor used for input match. The maximum available gain and the minimal noise figure are also included in the figure. These values were determined using the nominal beta. Simulation indicates that the maximum available gain is 14.7dB and the minimal noise figure is 3.6dB, indicating that noise figure goal is possible but the gain will fall short of the 15dB goal. This is the same case for LNA2 having a maximum available gain of 14.4dB and minimal noise figure of 3.8dB.
Table 0.7: Comparing ‘RLCK’, ‘PEEC+LADDER’ and post LC adjustments for LNA1

<table>
<thead>
<tr>
<th>LNA1 Beta Adjusted</th>
<th>Peak Gain</th>
<th>Lowest NF</th>
<th>Best Input Match</th>
<th>Best Output Match</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1.1.0.0HP Simulated (Input1)</td>
<td><a href="mailto:12.8dB@19.2GHz">12.8dB@19.2GHz</a></td>
<td><a href="mailto:4.2dB@15.8GHz">4.2dB@15.8GHz</a></td>
<td><a href="mailto:-30.3dB@15.4GHz">-30.3dB@15.4GHz</a></td>
<td><a href="mailto:-13.8dB@19.7GHz">-13.8dB@19.7GHz</a></td>
</tr>
<tr>
<td>PEEC+LADDER Options (Input1)</td>
<td><a href="mailto:10.8dB@18.1GHz">10.8dB@18.1GHz</a></td>
<td><a href="mailto:4.4dB@17.3GHz">4.4dB@17.3GHz</a></td>
<td><a href="mailto:-16.9dB@15.8GHz">-16.9dB@15.8GHz</a></td>
<td><a href="mailto:-8.1dB@18.6GHz">-8.1dB@18.6GHz</a></td>
</tr>
<tr>
<td>Flatten rline and C Adjustment (Input1)</td>
<td><a href="mailto:11.2dB@18.0GHz">11.2dB@18.0GHz</a></td>
<td><a href="mailto:4.5dB@19.7GHz">4.5dB@19.7GHz</a></td>
<td><a href="mailto:-19.3dB@19.3GHz">-19.3dB@19.3GHz</a></td>
<td><a href="mailto:-7.1dB@18.1GHz">-7.1dB@18.1GHz</a></td>
</tr>
<tr>
<td>Measured Input1 Data</td>
<td>10.4dB@18GHz</td>
<td><a href="mailto:5dB@19.56GHz">5dB@19.56GHz</a></td>
<td><a href="mailto:-19.47dB@19.5GHz">-19.47dB@19.5GHz</a></td>
<td><a href="mailto:-7.05dB@18.1GHz">-7.05dB@18.1GHz</a></td>
</tr>
<tr>
<td>V1.1.0.0HP Simulated (Input2)</td>
<td><a href="mailto:13.6dB@19.2GHz">13.6dB@19.2GHz</a></td>
<td><a href="mailto:4.2dB@16.6GHz">4.2dB@16.6GHz</a></td>
<td><a href="mailto:-38.5dB@16.0GHz">-38.5dB@16.0GHz</a></td>
<td><a href="mailto:-13.8dB@19.7GHz">-13.8dB@19.7GHz</a></td>
</tr>
<tr>
<td>PEEC+LADDER Options (Input2)</td>
<td><a href="mailto:10.3dB@18.0GHz">10.3dB@18.0GHz</a></td>
<td><a href="mailto:4.4dB@16.8GHz">4.4dB@16.8GHz</a></td>
<td><a href="mailto:-17.8dB@15.9GHz">-17.8dB@15.9GHz</a></td>
<td><a href="mailto:-8.6dB@18.7GHz">-8.6dB@18.7GHz</a></td>
</tr>
<tr>
<td>Flatten rline and C Adjustment (Input2)</td>
<td><a href="mailto:10.8dB@17.9GHz">10.8dB@17.9GHz</a></td>
<td><a href="mailto:4.7dB@19.6GHz">4.7dB@19.6GHz</a></td>
<td><a href="mailto:-22.5dB@18.6GHz">-22.5dB@18.6GHz</a></td>
<td><a href="mailto:-7.6dB@18.0GHz">-7.6dB@18.0GHz</a></td>
</tr>
<tr>
<td>Measured Input2 Data</td>
<td>9.8dB@18GHz</td>
<td><a href="mailto:5.4dB@19.56GHz">5.4dB@19.56GHz</a></td>
<td><a href="mailto:-21.96dB@18.6GHz">-21.96dB@18.6GHz</a></td>
<td><a href="mailto:-7.2dB@18.1GHz">-7.2dB@18.1GHz</a></td>
</tr>
</tbody>
</table>

Figure 0.8: LNA1, Input2 simulations using the latest design kit and extraction deck. rline uses the inductor model in the design kit. ‘flatten rline’ had the inductors extracted before simulation.
5.4 LNA1 and LNA2 Extraction Comparison

It has been shown that it is required to use all of the options available within the Assura tool, as described in Appendix A, to get an accurate netlist of the parasitic components at this frequency of operation. Use of these options is constrained by the computational resources needed to extract and simulate the given area of the layout. It is possible to divide the layout into sections to extract and analyze a section at a time and then combine them.

The models available in the design kit allow faster extraction and simulation times, but care is required in the layout of these models. Table 5.8 provides easy comparison between the two layouts’ matching components and the changes required to approximate the measured data. All input matching inductors in both designs were approximately 24% less inductance than the model indicated. The inductor model assumes all ground return current to be in the substrate. The model guide states that all substrate contacts to be at least 50um away from the rfline, but 80um is suggested. This was done, but it is shown in Appendix A that the return ground on layer M1 at 26.5um away from the inductor metal conducted enough of the ground return to cause significant variations from the ideal model. The output matching inductors for both designs abided by the rules and have the return ground metal further than 80um away from the inductor, so the model should have been accurate, but here the model underestimated the inductance. The same study in Appendix A done for the input matching inductors was done for the output matching inductor layout used in LNA1. The results shows that the further away the metal for the return current is from the inductor metal, the higher the actual inductance and resistance when compared to the model. The results were found by
removing the pcell identity of the output matching inductors and extracting the layout using the proper setup in the Assura tool as explained in Appendix A. This was compared to the Momentum results. Both tools captured the inductance within reasonable accuracy for LNA1. Conversations with the IBM research center [20], who are using the 8HP design kit for 60GHz applications, indicated that they had issues predicting the inductance due to it’s relying on a variable substrate resistance for the return currents. Their suggestion is to use the singlewire or a coplanar waveguide for inductors so there is a better define path for the return currents. The drawback of this would be a longer line length would be required. Another option would be to include the return current metal in the pcell where the user defines which metal layout to use.

The transmission line model singlewire appears accurate in the latest design kit, but comparing the latest design kit extraction results to the original show that the original extraction techniques indicated no modeling of the parasitic interactions between the model, the connecting return ground and any nearby metals. This is evident by comparing the adjustments needed on the matching elements to align the measured results to the simulation results of the two design kits for LNA1. Table 5.8 list the value of the matching components for LNA1 and LNA2 for both design kits for comparison. The required adjustment for the input matching capacitors for LNA1 required less than 10% adjustment in the latest design kit compared to >45% for the original design kit.
Table 0.8: Comparing the value of matching components required for matching LNA1 and LNA2. ‘RLCK’ is the original values determined from the extraction using the standard ‘RLCK’ method. PEEC(1) is the values required to match measured data after extracting using the original design kit. PEEC(2) is the values required to match measured data after extracting using the latest design kit.

<table>
<thead>
<tr>
<th>LNA1 Matching Component</th>
<th>‘RLCK’</th>
<th>PEEC(1)</th>
<th>% Change</th>
<th>PEEC(2)</th>
<th>% Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input1 Inductor (pH)</td>
<td>440</td>
<td>313</td>
<td>-28.86</td>
<td>325</td>
<td>-26.1</td>
</tr>
<tr>
<td>Input1 Capacitor (fF)</td>
<td>140</td>
<td>212</td>
<td>51.43</td>
<td>180</td>
<td>8.0</td>
</tr>
<tr>
<td>Input2 Inductor (pH)</td>
<td>440</td>
<td>331</td>
<td>-24.77</td>
<td>338</td>
<td>-23.2</td>
</tr>
<tr>
<td>Input2 Capacitor (fF)</td>
<td>140</td>
<td>206</td>
<td>47.14</td>
<td>182.2</td>
<td>9.1</td>
</tr>
<tr>
<td>Output Inductor (pH)</td>
<td>589</td>
<td>672</td>
<td>14.09</td>
<td>672</td>
<td>14.0</td>
</tr>
<tr>
<td>Output Capacitor (fF)</td>
<td>57.24</td>
<td>53</td>
<td>-7.41</td>
<td>59</td>
<td>3.1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>LNA2 Matching Component</th>
<th>‘RLCK’</th>
<th>PEEC(1)</th>
<th>% Change</th>
<th>PEEC(2)</th>
<th>% Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input1 Inductor (pH)</td>
<td>410</td>
<td>301</td>
<td>-26.37</td>
<td>315</td>
<td>-23.17</td>
</tr>
<tr>
<td>Input1 Capacitor (fF)</td>
<td>187.9</td>
<td>188</td>
<td>2.1</td>
<td>188</td>
<td>1.84</td>
</tr>
<tr>
<td>Input2 Inductor (pH)</td>
<td>410</td>
<td>301</td>
<td>-26.37</td>
<td>315</td>
<td>-23.17</td>
</tr>
<tr>
<td>Input2 Capacitor (fF)</td>
<td>187.9</td>
<td>188</td>
<td>2.1</td>
<td>188</td>
<td>1.84</td>
</tr>
<tr>
<td>Output Inductor (pH)</td>
<td>389</td>
<td>477.7</td>
<td>22.80</td>
<td>473</td>
<td>21.59</td>
</tr>
<tr>
<td>Output Capacitor (fF)</td>
<td>198.65</td>
<td>214.7</td>
<td>8.1</td>
<td>213.75</td>
<td>7.60</td>
</tr>
</tbody>
</table>
CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 Contributions

This work shows that it is possible to eliminate the traditional switch while keeping the capability to switch between multiple ports in the required amount of time, maintain isolation, and have both inputs track each other over temperature and supply voltage variations. In addition, these designs used SiGe BiCMOS technology instead of GaAs, which is 3 times cheaper to fabricate than GaAs for similar HBT performance [21]. Having the control circuit and merging the switching capability on the same layout produced a die that is 2.98 times smaller than the traditional method equating to a total savings multiplier of 8.94.

It did not meet the required gain and noise figure parameters due to low beta from the process and higher than expected transmission line loss and shift in matching resonance. The latter occurred because the extraction tool setup oversimplified the extraction of the self and mutual inductance of the ground and nearby metals, and the model for the inductor is too sensitive to the ground return path through the substrate.

Table 6.1 list the parameter goals and compares the two designs presented here to the traditional method of using a switch plus an LNA for the front end of the radiometer presented in Chapter 2. The goal numbers not met are in red. The presented designs consumes an order of magnitude less power than the traditional method and close to 50% less die area. Another advantage is that this design requires only positive 2.25VDC and 1.5VDC voltage supplies compared to the 3.5VDC and -1.0VDC supply required by the...
GaAs LNA. Switching the ports of this design requires one 0/1.5V control line compared to the switch requiring two lines supplying either 0VDC or -5.0VDC. The conventional switch and LNA has a 4dB higher input P1dB and a factor of eight faster switching times, greatly exceeding any radiometer requirements. The gain and noise figure are two important parameters where the conventional current switch and LNA performs better than the designs presented in this thesis.

**Table 0.1:** Parameter list to compare LNA1 and LNA2 to the traditional Switch+LNA design approach.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Goal</th>
<th>Switch+LNA</th>
<th>LNA1 (In#1)</th>
<th>LNA1 (In#2)</th>
<th>LNA2 (In#1)</th>
<th>LNA2 (In#2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency Band</td>
<td>18.7GHz-19.3GHz</td>
<td>18.7GHz-19.3GHz</td>
<td>17.7GHz-18.3GHz</td>
<td>16.3GHz-16.9GHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Noise Figure</td>
<td>&lt;4.15dB</td>
<td>4.15dB</td>
<td>5.5dB</td>
<td>5.2dB</td>
<td>5.2dB</td>
<td>5.2dB</td>
</tr>
<tr>
<td>Gain</td>
<td>&gt;15dB</td>
<td>15.5dB</td>
<td>10.4dB</td>
<td>9.8dB</td>
<td>10.0dB</td>
<td>9.4dB</td>
</tr>
<tr>
<td>Gain Flatness (In Band)</td>
<td>&lt;0.5dB</td>
<td>0.1dB</td>
<td>0.1dB</td>
<td>0.1dB</td>
<td>0.23dB</td>
<td></td>
</tr>
<tr>
<td>ΔGain vs. Temperature</td>
<td>&lt;[0.1dB]/˚C</td>
<td>Not Available</td>
<td>-0.002dB/˚C</td>
<td>Not Measured</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input P1dB</td>
<td>&gt;-40dBm</td>
<td>-9.4dBm</td>
<td>-10.1dB*(in)</td>
<td>-13.2dB*(out)</td>
<td>-12.8dB*(in)</td>
<td>-11.18dB*(out)</td>
</tr>
<tr>
<td>Return loss on all ports</td>
<td>&lt;-12dB</td>
<td>-8.5dB*(input of LNA)</td>
<td>-10.1dB*(in)</td>
<td>-13.2dB*(out)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Isolation: 'Off' input to output</td>
<td>&gt;35dB</td>
<td>35dB</td>
<td>34dB</td>
<td></td>
<td>45dB</td>
<td></td>
</tr>
<tr>
<td>Isolation: 'Off' input to 'On' input</td>
<td>&gt;35dB</td>
<td>43dB</td>
<td>47dB</td>
<td>45dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switching times</td>
<td>&lt;5us</td>
<td>6ns</td>
<td>48ns</td>
<td>48ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Consumption</td>
<td>&lt;<a href="mailto:60mA@3.5VDC">60mA@3.5VDC</a></td>
<td>60mA to <a href="mailto:100mA@3.5VDC">100mA@3.5VDC</a></td>
<td><a href="mailto:8.8mA@2.25V">8.8mA@2.25V</a></td>
<td>19.8mW</td>
<td><a href="mailto:8.8mA@2.25V">8.8mA@2.25V</a></td>
<td>19.8mW</td>
</tr>
<tr>
<td>Die Size</td>
<td>Smallest possible</td>
<td>(3.37 x 1.83)=6.17mm^2</td>
<td>(1.83 x 1.13)=2.07mm^2</td>
<td>(1.71 x 1.2)=2.05mm^2</td>
<td></td>
<td></td>
</tr>
<tr>
<td># of supplies and control lines</td>
<td>NA</td>
<td>4</td>
<td>3</td>
<td>3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* Includes wirebond model.

It is highly questionable if the gain could achieve the required 15dB after the updated models and extraction deck with the proper setup, which better correlate with the measured data, indicate that the maximum available gain is 14.7dB. This gain is achievable if the process achieves the nominal beta of 600. Input#1 measured gain of LNA1 would have improved to 12.8dB if process met the specified beta. Adding the
wirebonds would have improved it by 0.5dB giving a total gain of 13.3dB. Looking at LNA2, the measured gain would have been improved to approximately 12.4dB if process met the specified beta. Proper matching, mostly of the output, would have moved the peak gain from 16.9GHz to 19GHz and increased it to 13.03dB. The two designs fall short by about 2dB.

Increasing current would increase the gain but also the noise figure, which is already high. Using different size transistors do not provide any advantages in gain versus noise figure looking at figures 3.9 and 3.10. These figures show that setting a collector current for a given size transistor will provide ‘X’ amount of maximum gain and ‘Y’ amount of minimum noise figure; Using a different size transistor with a collector current to provide ‘X’ amount of maximum gain will also provide the same minimum noise figure.

The measured noise figure result is 5.2dB, which is 1dB over the limit. Noise figure failed primarily because of line loss and added noise from coupling from the substrate and return ground between the input stage, including the matching circuitry, to the common base stage, not due to the low beta or the shift in the matching circuitry.

The minimum noise figure at 19GHz for this transistor is 1.3dB for both the common emitter and common base configuration. Lowering the beta to 287 slightly increases minimum noise figure increases to 1.4dB. The high gain of the first stage nulls the noise contribution of the second stage.

The frequency shift in the matching circuitries did increase the minimum noise figure by 0.2dB for both designs, but it had little effect on the expected noise figure at 19Ghz. The shift in resonance of the input matching circuitry in both designs to a higher
frequency moved the minimal noise figure from the low 17GHz range to the 19GHz range, so instead of expecting 4.8dB (using the PEEC extraction) on the high end of the noise figure bell curve, the measurement took place at the minimum noise figure where the PEEC extraction indicated 4.7dB at 19GHz.

The majority of the noise lies in the line loss, which was captured after improvement in the singlewire model and using the proper extraction technique that creates the equivalent circuits for the hand drawn metals. This is evident by comparing the tables in Chapter 5 where the improved singlewire model in the V1.1.0.0HP kit captured an additional 1.0dB of noise figure for LNA1 increasing it from 3.2dB to 4.2dB. Adding the PEEC option to capture the input circuitry for this design added an additional 0.2dB. LNA2 didn’t use the singlewire model so its noise figure of 3.2dB did not change when the models were upgraded to the newer version. Instead the modeling of it’s interconnect lines rely entirely on the proper setup of the extraction tool. Engaging the PEEC option captured an additional 1.4dB of noise figure for LNA2 increasing it from 3.2dB to 4.4dB.

Chapter 5 proved that the latest design kit transmission lines allow the extraction tool to capture return ground interactions. Chapter 5 also proved that the inductor model rfline is very sensitive to how the metal is laid out for the current return even if placed further than the 50um specified in the design manual. Overall this chapter showed that the simulations will closely approximate the measured data by setting up the proper the extraction options.
6.1.1 Future Work

Future work would start with determining if the gain and noise figure requirements could be met by reanalyzing the interactions between the transistors, the matching circuitry and the transmission lines; primarily the ground layout around the input section from the I/O pad to the common emitter stage and the connection between Q1, Q2 and Q3. The ground layout was done with the intention of maintaining isolation between the two inputs. However, the lack of ground appears to be responsible for majority of the gain reduction and added noise figure. This is proven by comparing LNA2 gain and noise figure RLCK extractions to the PEEC extractions. The 2.6dB gain reduction and 1.3dB noise figure increase going from ‘ideal’ ground to the extracted ground shows the effect that the ground layout has on gain and noise figure. The PEEC ‘user regions’ for LNA1 consisted primarily of the input stages because the rest of the layout was modeled by design kit elements rfline and singlewire. This design’s noise figure increased only 0.2dB when comparing ‘RLCK’ to the ‘PEEC’ extraction.

The maximum available gain and minimal noise figure indicates that the gain and the noise figure can not be compensated by different matching alone without changing the layout and or matching topology. Another focus would be to see if reducing the length of the input lines is possible while maintaining the required 50um distance from the inductors, or use shorted coplanar waveguide or shielded microstrips instead of the inductors.

The transmission line model singlewire greatly reduces the extraction and simulation time compared to a manually laid out a transmission line for reasons explained in Appendix A. It also saves time in the design itself since it comes into the layout.
predefined by the user. This model, shown to accurate in the latest design kit, will be preferred in the next design to decrease design time in reevaluating the ground layout.

Another possible option for this design is to use cheaper silicon FET technology instead of SiGe bipolar devices. Several advancements in silicon FET technology have been achieved since the initial time of this study. 65nm technology is readily available and 45nm will be soon. It is expected that 32nm technology will be available within the next two years. All of these technologies also setup for analog applications as well offering similar passive components presented in this study along with additional inductor designs.

This study focused on using the ‘switching cascode’ for the given radiometer application. Another possible use would be for multiband applications such as cellular. Typical multiband phone designs have one LNA for each band tied to a common switch. Often the output of these LNA’s is tied to a common mixer because the mixers are broadband. An LNA for each band is required because its input needs to have its noise figure with gain optimized for that frequency. This methodology would allow eliminating the switch while still achieving optimal tuning for that input band. Both high performance bipolar and FET transistors, having high output resistance and low reactance at these cellular frequencies, allows easier broadband matching for the output. This design could also be expanded to allow more than two inputs. The cellular frequencies being much lower than this study, will allow easier implementation in achieving multiple inputs, the required gain, noise figure, return losses and isolation. Achieving the required switching speeds also will need to be studied. A quick study was done for the 900MHz and 1800MHz bands as shown in Appendix F. This study shows that 24dB of gain and
1.45dB of noise figure can be achieved for the 900MHz band, and 22dB of gain and
1.4dB of noise figure can be achieved for the 1.8GHz band. All return losses are better
than 10dB. It is expected that better noise figure and return losses can be obtained with
better matching analysis. Worse case isolation still exceeds 70dB.
APPENDIX A

ASSURA EXTRACTION

The Assura tool is the Design Rule Checking (DRC), Layout Versus Schematic (LVS) and parasitic extraction tool (RCX) supporting the IBM BiCMOS8HP design kit. This appendix focuses on the options within the RCX portion available to the user and how these options are applied to the two designs presented in this paper. The last section does a study on the inductors used to match the LNA to compare the RCX results to that of the Agilent’s EM simulator Momentum.

Setup

The Assura extraction tool like many extraction tools require performing a layout versus schematic (LVS) run before extraction is performed so netlists of the layout can be compared to the schematic to ensure proper connections. This netlist is used for the extraction tool to build parasitic components in the netlist as dictated by the extraction setup. The setup possibilities for this tool consist of resistance only, capacitance only or both. In addition, this tool allows the user to extract out self and mutual inductances. Resistance due to skin effect can also be taken into account. The highest frequency of operation is required so the tool knows how small to make the divisions in metal length and coupling distance to determine accurate resistance, capacitance and inductance. The minimum value extracted for these parasitic components are setup by the user or the default can be used. So if the tool calculates a resistance or capacitance value that is smaller than specified in the GUI by the designer, it is ignored. Thus the number of parasitic components generated from the layout increases with the user defined operating
frequency, the lower the defined minimum value for the parasitic component, and the
density and size of the chip. This means a balance must be made between accuracy of the
simulation and the capability of the computer. Higher accuracy requires more memory
and computation time.

The resistance and capacitance extraction (RC) works like most extraction tools in
that it places a resistance (DC value) at each intersection or at locations in a polygon that
exceeds a maximum specified fracture length. Parasitic capacitors are placed at the same
nodes to form an RC network. The capacitors generated at these nodes must meet the
minimum capacitance defined value and fit the selected ‘Cap Extract Mode’: Coupled,
Decoupled or Decoupled to Substrate. Coupled means capacitors are defined between
the nets defined by the user. Capacitance that exists between selected nets and non-
selected nets are defined by capacitance connecting to a common reference net, also
defined by the user; usually ground. Decoupled means all nets defined or not, are
coupled to the defined common reference net. Decoupled to Substrate means all nets are
decoupled to the substrate ground specified to the area that the parasitic capacitor occurs
in the design.

The inductance extraction is more complex in setup. The user can select just to
do ‘RLC’ extraction which is resistance, capacitance and self inductance extraction, or do
‘RLCK’ extraction which is the same with the addition of mutual inductance. Typically
if inductance is a concern, then the full RLCK extraction is suggested. There are three
combinations the user can select when using RLC or RLCK extraction to determine self
and mutual inductance of a net. They are: Default, Partial Element Equivalent Circuit
(PEEC) and LADDER. All options divide nets in the layout at every 45 and 90 degree bend of metal to determine capacitance and dc resistance.

Using the default option extracts inductance using a return-limited inductance method which output loop inductance values. It assumes that all power and ground networks (defined by the user) have low impedance and are available for current return. It also assumes that the current return collapses around the signal wire. These two assumptions means the net is bounded by the nearest ground or power net. If two signal nets are next each other, then they may return on each other’s net. These loop inductance values are called current-limited loop inductance. No inductance values are assigned to, or between power or ground nets since they are already incorporated into the loop inductance of the signal lines. This option keeps the number of inductor components low so it allows a large chip area to be extracted.

The PEEC option does not make the assumption that the power and ground nets are ideal so they are treated the same as the signal nets. It also looks at the highest frequency of operation specified so to determine how to divide the polygon shapes instead of only at bends. This can generate a large number of inductor components. Because of this, the user must select what areas of the layout need to be considered for inductance extraction called user regions. In addition, the user can name the specific nets within the user regions. Different user regions can abut but not overlap. Mutual inductances will be extracted for nets within a user region but not between nets in different user regions. It is also important to the ‘Max fracture length’ to be less than infinite for inductance extraction.
Adding the LADDER option takes into account skin effect and proximity effects. The latter is dependent on nearby conductors and the relative phase of current within the wires. The skin effect is handled by generating as series inductor and resistor tied to a resistor in parallel with an inductor. The resistor in parallel to the inductor acts as the skin effect resistance. The inductors can be mutually coupled to nearby inductors to model the proximity effect. The placement of these ladder networks occurs where the RLCK extraction determines where each inductor net is defined so it is suggested that it is used in conjunction with the PEEC option, which was not done for the prefabrication simulations in section 3.6.2. The accuracy of these nets is rated from DC to 50GHz.

The IBM 8HP design kit also has a substrate file that allows the user to use Substrate Extract option in Assura. This option extracts parasitic resistance and capacitances within areas of the substrate defined by the user called bBoxes. Typically areas containing the active microwave FETs are selected. This option automatically selects the PEEC mode. More information about this tool can be found in the Assura Physical Verification User Guide. The substrate file for this technology is available only for internal use and specific customers. Help by the lead IBM Assura extraction engineer was required to properly set it up [18].

It is important to know that independent of what combination of options are chosen, components such as singlewire, MIM cap and rфline are already modeled so the extraction tool points to the model instead of ‘extracting’ it. This can greatly reduces the extraction files size so therefore decrease simulation times substantially, but it could also miss critical coupling effects. Accuracy of the models is always important. A case in point of this is to compare the two layouts: LNA1 and LNA2. Layout LNA1 shown in
Figure A.1 shows the regions where PEEC and LADDER extractions were done. Note that the *singlewire* and *rfline* components were not selected because they would not be extracted. Larger areas of the return ground on layer M1 for the matching inductors were selected and extracted, but no differences were noticed in the simulations. The numbers of parasitic components generated for the shown regions for the different methods of extractions are listed in Table A.1. S-parameter simulation times are also compared in this table. Extraction times are not included in the table but all but the last option was less than 5 minutes. Adding the LADDER option added another 10 minutes for this layout.

**Figure A.1:** LNA1 Layout Showing *User Regions* for PEEC extraction.
**Table A.1:** Parasitic Components Extracted and Simulation Times vs. Extractions Method for LNA1.

<table>
<thead>
<tr>
<th>Extraction Method</th>
<th>Resistors</th>
<th>Capacitors</th>
<th>Self Inductors</th>
<th>Mutual Inductors</th>
<th>15-22GHz S-parm Sim Times</th>
</tr>
</thead>
<tbody>
<tr>
<td>RC</td>
<td>1079</td>
<td>1517</td>
<td>NA</td>
<td>NA</td>
<td>10 seconds</td>
</tr>
<tr>
<td>RLCK (Default)</td>
<td>1029</td>
<td>1671</td>
<td>173</td>
<td>994</td>
<td>15 seconds</td>
</tr>
<tr>
<td>RLCK (PEEC)</td>
<td>10426</td>
<td>5959</td>
<td>539</td>
<td>18030</td>
<td>2 minutes</td>
</tr>
<tr>
<td>RLCK (PEEC + Substrate)</td>
<td>10426</td>
<td>11625</td>
<td>539</td>
<td>18030</td>
<td>2.5 minutes</td>
</tr>
<tr>
<td>RLCK (PEEC + Substrate + LADDER)</td>
<td>10731</td>
<td>11625</td>
<td>843</td>
<td>25680</td>
<td>4.5 minutes</td>
</tr>
</tbody>
</table>

LNA2 layout showing the *User Regions* is shown in Figure A.2. Similar areas to LNA1 were selected along with a portion of the transmission line going to the output. No *singlewire* transmission lines were used in this layout so it was important to try to capture inductance and skin effect of these lines. A larger selection of the outgoing transmission line was tried but the amount of components generated was too much for a Linux 32 bit computer to simulate. For the same reason, another extraction was performed on the transmission lines connecting the two common emitter transistors to the common base transistor (not outlined), so a rough calculation could be made to determine the phase shift and resistance connecting these transistors.

Table A.2 list the numbers of parasitic components generated for the shown regions per extraction method. Simulation times are also included for comparing to LNA1. It is evident that using the component *singlewire* reduces the number of parasitic components and simulation time substantially. Extraction also takes longer when including all options. The extraction time for LNA2 took less than 5 minutes for RC and RLCK-default option, 20 to 25 minutes for RLCK + PEEC and RLCK+PEEC+Substrate respectfully and 4 hours when the LADDER option was included.
Figure A.2: LNA2 Layout Showing User Regions for PEEC extraction.

Table A.2: Parasitic Components Extracted and Simulation Times vs. Extraction Method for LNA2.

<table>
<thead>
<tr>
<th>Extraction Method</th>
<th>Resistors</th>
<th>Capacitors</th>
<th>Self Inductors</th>
<th>Mutual Inductors</th>
<th>15-22GHz Sim Times</th>
</tr>
</thead>
<tbody>
<tr>
<td>RC</td>
<td>1701</td>
<td>1912</td>
<td>NA</td>
<td>NA</td>
<td>30 seconds</td>
</tr>
<tr>
<td>RLCK (Default)</td>
<td>1548</td>
<td>2162</td>
<td>233</td>
<td>1797</td>
<td>1 minute</td>
</tr>
<tr>
<td>RLCK (PEEC)</td>
<td>30313</td>
<td>8651</td>
<td>1327</td>
<td>126,380</td>
<td>35 minutes</td>
</tr>
<tr>
<td>RLCK (PEEC + Substrate)</td>
<td>30313</td>
<td>11625</td>
<td>1327</td>
<td>126,380</td>
<td>40 minutes</td>
</tr>
<tr>
<td>RLCK (PEEC +Substrate + LADDER)</td>
<td>31321</td>
<td>11625</td>
<td>2223</td>
<td>211,409</td>
<td>5.5 hours</td>
</tr>
</tbody>
</table>

Simulation times are important but the accuracy of these extractions is more important. How the extraction methods compare to the EM simulator Momentum is discussed next.
Assura and Momentum Compared

Analyzing the input match for designs LNA1 and LNA2 in Chapter 5 show that input matching inductors \textit{rline} effective length was shorter than modeled; 318pH vs. 440pH for LNA1, and 315pH vs. 410pH for LNA2. Likewise, analyzing the output match for these designs show that the output matching inductors effective length was longer than that modeled; 671.8pH vs. 589pH for LNA1 and 473pH vs. 389pH for LNA2.

It was shown in section 3.5.1 that the ‘RLCK’ extraction of the inductor layout and that done in ADS agree. After further study of how the Assura tool extracts inductance as provided in this appendix, the layout in ADS was revisited to better understand why it too over estimated the inductance used for matching the input. It will be shown that the ground return on metal M1 in the layout had more effect than initially expected. This was overlooked because of the close agreement that the two simulations had in section 3.5.1.

A new study was done to see if these inductors could be accurately modeled if the current return path and the 5pF MIM capacitor were included in the ADS tool like that in the actual layout. The first study was on the input matching inductor circuit of LNA1 seen in Figure A.3. The second study was on the output matching inductor circuit of LNA1 seen in Figure A.4. The extraction setup for these layouts included the RLCK PEEC option encompassing the full layout and the maximum fractured length was set at 20um. It is important to include the substrate file for this extraction, particularly for the output matching inductors, which depend more on the substrate for the return current having their ground metal further away. The extraction was then simulated using Spectre.
using an option to produce a touchstone format file so it could be imported into the Agilent ADS tool so comparisons could be made with the Momentum results.

Momentum simulations were done by first copying these layouts, including the substrate, metal, vias and dielectric properties and then simulated. The primary difference between the Spectre and Momentum simulations is the MIM capacitors had to be removed for Momentum because of lack of spacing information between the two metal plates of the MIM capacitor. However, the top metal (AM) that connected all the MIM capacitors and the connections from the bottom plate to the ground metal was included. This required using twelve ports in Momentum: Port 1 at the input of the inductor with its reference port connecting to the ground metal M1 underneath it, and one port along with its reference port placed at where each of the five 1pF MIM capacitors are connected. This simulation produced a 6 port s-parameter file because the reference ports were combined with their associated port. The 6 port s-parameter file that was brought into the schematic tool and simulated with a 50 Ohm port connected to port 1 and a 1pF capacitor connected to ports 2 through 6. A simple 1pF capacitor representing the MIM capacitors was considered accurate enough after analyzing results in Chapter 4 compared to the required matching adjustments in Chapter 5.
The results from these simulations produced a one port S11 file. A Smith chart comparing the Assura and Momentum results for the input matching inductor are shown on the left in Figure A.5. The results for the output matching inductor are shown on the right side in this figure. Comparison shows that the two methods are within 1% agreement of each other for the input and output matching circuits. The input matching inductor having a reactance of 38 Ohms at 19GHz equates to 318pH. 318pH is within 3% of the 325pH value determined iteratively. The Q of this circuit is 11.9, about 2.6 times less than the inductor model predicts. This result shows that having the return ground metal closer than 50um away from the inductor metal will decrease the effective length compared to the model.
The output matching inductor having a reactance of 80.5 Ohms at 19GHz equates to 674.6 pH. 674.6pH is less than 1% difference of the 671.8pH value determined iteratively. The Q of this circuit is approximately 8.1, about 2.3 times less than the inductor model predicts. The Q is degraded slightly by the use of the more accurate MIM capacitor model. This result shows that having the ground metal at 75um away has the opposite effect on the effective length. This study along with the one done in 3.5.1 shows that the rfline model is most accurate when the return ground metal surrounds the inductor metal at a distance of 50 to 60um. This dependency indicates that the rfline pcell should include the return ground metal to improve its accuracy.

**Figure A.5:** Simulation results comparing Assura extraction of matching inductor circuits to Agilent’s Momentum. $S(1,1)$ is the Momentum result for the input matching inductor circuit shown in figure A.3. $S(3,3)$ is the Spectre result from the Assura extraction for the input matching inductor circuit. $S(2,2)$ is the Momentum result for the output matching inductor circuit shown in figure A.4. $S(4,4)$ is the Spectre result from the Assura extraction for the output matching inductor circuit.
APPENDIX B

BONDWIRE

Designing the bondwires was done using the Agilent’s ADS2005A tool. There are several features within this tool to do the design. The first feature is the component ‘BONDWn’ located in both the schematic and layout windows. This model developed by Philips and TU Delft allows the user to specify the number of bondwires to model from 1 to 50 in the form ‘BONDWn,’ where n is the number of bondwires. This model can break down the bondwire up into five straight segments to form the bondwire shape. This shape is defined by either ‘BONDW_Shape’ or ‘BONDW_Usershape,’ which allows the user to define the shape, or curvature, of the wire. Figure B.1 shows an example of the parameters that are defined by the ‘BONDW_Shape.’ It assumes a ground plane and the tilt angle decides if to use three line segments or five.

‘BONDW_Usershape’ provides more flexibility for the designer as shown in Figure B.2. It always consists of five line segments and no ground plane is assumed. A number of different shapes can be defined depending on the design requirements. The BONDWn together with the shape models determines self and mutual inductance between the bondwires. It does not consider coupling capacitance between them, but it does determine capacitance between the wires and the ground plane. More information on these models such as what math models that they are based can be found in the Agilent’s ADS user help guide.
This design required only one shape; ‘BONDW_Shape’ for each of the ground-signal-ground (GSG) wires since they all were going to be shaped identically. Figure B.3 shows the Ground-Signal-Ground wirebond model used to characterize the wirebond
inductance. The shape is defined as a 25mil diameter wire that starts and end at the same height of 200um above the ground plane. This will occur if the board material has 5mils of dielectric thickness between the transmission line and its ground. The die back grounded to a thickness of 200um will set in a cutout of the board so the die surface is at the same level of the transmission line. A four wire model, ‘BONDW4,’ was used to simulate the wire connection between the die GSG pads and the board, where bondwire #1 and #4 connect the two ground pads and bondwire #2 and #3 form two parallel wires connecting to the signal pads. This is done by setting the parameter “SepY” to equal 125um. Each of the four wires is then separated in this direction by 125um with wire #1 being ground at Y=0. To get wire #3 on the same pad as #2, which is centered at Y=125um, ‘W3_Yoffset’ is set to equal -105um to bring it to Y = (250 -105) = 145um. Wire #2 has ‘W2_Yoffest’ to equal -20um so it sits at Y = (125-20) = 105um. They now sit on the same signal pad that is 100um wide. The ground wire #4 has its ‘W4_offset’ equal to -125um so it sits at Y = 250um. Note that they all point to “Shape1” and their conductivity is set to that of gold.

**Figure B.3:** Ground-Signal-Ground Wirebond Schematic Model.
An s-parameter simulation was done for this setup from 18GHz to 20GHz. Plotting the Smith chart, shown in Figure B.4, indicates that this wirebond setup has an inductance of 152pH.

![Smith Chart](image)

**Figure B.4:** Smith Chart showing results from the Bondwire model in Figure B.3.

Ribbon wire is another option that was considered for connecting the die to the board. There are no schematic models to emulate ribbon wire so the Agilent’s ADS tool Momentum was used to simulate it. Figure B.5 shows a layout of GSG ribbon wire. The substrate was defined as air 200um thick between the ribbons and a ground plane underneath them. Ports P1 and P2 are the signal ports, ports P3 and P4 are the ground reference for port P1, and ports P5 and P6 are ground reference for P2.

The Smith chart in figure B.6 shows that a gold ribbon wire that is 80um wide and 20um thick will provide 156pH inductance if the length is 550um.
Figure B.5: 125um pitch GSG layout of 550um long, 80um wide and 20um thick gold ribbon wire.

Figure B.6: Smith chart results for the GSG ribbon wire shown in Figure B.5.
APPENDIX C

LNA1 SIMULATION PLOTS

The following plots are for layout LNA1 that were not shown in the main text. The plots start with the most important of these plots which compare the symmetry between input 1 and input 2. Only the RLCK extractions were done for comparison plots since it was taken to be accurate. Simulations not having the wirebond matching are included so comparisons can be made to the measured results.

Some plots compare the simulated results for the schematic and all four layout extracted models. The “schematic” curve is the result from changing the matching component values in the schematic to the values required to match in the layout. This was necessary when running the layout versus schematic (LVS) function in the Cadence IC tool.
Figure C.1: LNA1 gain for Input 1 for all models with the wirebonds modeled.

![LNA1 Gain Diagram]

Figure C.2: LNA1 gain for Input#1 for all models without the wirebonds modeled.

![LNA1 Gain Diagram]

Figure C.3: LNA1 noise figure for Input#1 for all models with the wirebonds modeled.

![LNA1 Noise Figure Diagram]
Figure C.4: LNA1 noise figure for Input#1 for all models without the wirebonds modeled.

Figure C.5: LNA1, Input#1 reflection coefficient magnitude response with wirebonds.
Figure C.6: LNA1, Output reflection coefficient response with wirebonds.

Figure C.7: LNA1, Gain (isolation) simulation from Output to Input#1 (on).
Figure C.8: LNA1, Gain (isolation) simulation from Input#1 (on) to Input#2 (off).

Figure C.9: LNA1, Gain (isolation) simulation from Input#2 (off) to Input#1 (on).
Figure C.10: LNA1, Gain (isolation) simulation from Input#1 (off) to Output.

Figure C.11: LNA1, Gain (isolation) from Output to Input#1 (off).
**Figure C.12:** LNA1 gain comparison between Input 1 and Input 2 with the wirebond modeled.

**Figure C.13:** LNA1 gain comparison between Input 1 and Input 2 without the wirebond modeled.
Figure C.14: LNA1 noise figure comparison between Input 1 and Input 2 with the wirebond modeled.

Figure C.15: LNA1 noise figure comparison between Input 1 and Input 2 without the wirebond modeled.
Figure C.16: LNA1 input match comparison between Input 1 and Input 2 with the wirebond modeled.

Figure C.17: LNA1 input match comparison between Input 1 and Input 2 without the wirebond modeled.
Figure C.18: LNA1 output match comparison between Input 1 and Input 2 with the wirebond modeled.

Figure C.19: LNA1 output match comparison between Input 1 and Input 2 without the wirebond modeled.
Figure C.20: LNA1 output to input gain (isolation) comparison between Input 1 and Input 2 with the wirebond modeled.

Figure C.21: LNA1 output to input gain (isolation) comparison between Input 1 and Input 2 without the wirebond modeled.
Figure C.22: LNA1 input match comparison between Input 1 and Input 2 when they are off with the wirebond modeled.

Figure C.23: LNA1 input match comparison between Input 1 and Input 2 when off without the wirebond modeled.
Figure C.24: LNA1 input to output gain (isolation) comparison between Input 1 and Input 2 when off with the wirebond modeled.

Figure C.25: LNA1 input to output gain (isolation) comparison between Input 1 and Input 2 when off without the wirebond modeled.
Figure C.26: LNA1 output to input gain (isolation) comparison between Input 1 and Input 2 when off with the wirebond modeled.

Figure C.27: LNA1 output to input gain (isolation) comparison between Input 1 and Input 2 when off without the wirebond modeled.
The following plots are with respect to Input 1 of LNA1 that are not shown in the main text.

**Figure C.28:** LNA1 input match for Input 1 without the wirebond modeled.

**Figure C.29:** LNA1 output match when Input 1 is on without the wirebond modeled.
Figure C.30: LNA1 gain (isolation) from output to Input 1 when on without the wirebond modeled.

Figure C.31: LNA1 gain (isolation) from Input 1, when on to Input 2, when off without the wirebond modeled.
Figure C.32: LNA1 gain (isolation) from Input 2, when off to Input 1, when on without the wirebond modeled.

Figure C.33: LNA1 gain (isolation) from Input 1, when off, to Output without the wirebond modeled.
Figure C.34: LNA1 gain (isolation) from Output to Input 1, when off, without the wirebond modeled.

Figure C.35: LNA1 1dB input compression point for Input 1 without the wirebond modeled.
Figure C.36: LNA1 1dB input compression point for Input 2 with the wirebond modeled.
APPENDIX D

LNA2 SIMULATION PLOTS

The following plots are for layout LNA2 that were not shown in the main text.
The plots start with the most important of these plots which compare the symmetry
between input 1 and input 2. Only the RLCK extractions were done for comparison plots
since it was taken to be accurate.

Figure D.1: LNA2 input reflection comparing Input#1 and Input2 when they are off.
Figure D.2: LNA2 gain (isolation) between the ‘off’ input to the ‘on’ input.

Figure D.3: LNA2 gain (isolation) between the ‘on’ input to the ‘off’ input.
Figure D.4: LNA2 input 1 dB compression point for Input1.

Figure D.5: LNA2 input 1 dB compression point for Input2.
APPENDIX E

TEST SETUP

The test setup for this project consisted of the following equipment:

1. Agilent 8720ES combined with Agilent N4418A: 4-port 50MHz to 20GHz S-parameter Network Analyzer.
2. Agilent N8975A with source 346C: Noise Figure Meter 10MHz to 26.5GHz
3. Agilent E4419B: 10MHz to 18GHz Power Meter
4. Rhode & Swartz Spectrum Analyzer: 10kHz to 26GHz.
5. Techtronix 4-port Oscilloscope: DC to 3GHz
6. Keithly power supplies
7. Fluke Multi Meter
8. Three Gore 3.5mm two feet long cables.
10. Different DC probe configurations
11. Cascade manual prober station with temper controlled chuck capable of -50°C to 200°C.

The 4-port network analyzer allowed measuring the 3-port LNAs simultaneously. It was calibrated down to the probe tips using the Cascade supplied ceramic substrate calibration structures. This setup was used to characterize the s-parameters during temperature analysis and switching.

The 1dB compression test was done by setting the network analyzer to 19GHz and adjusting the power to the LNA. The output power was measured by the network analyzer. The power was increased from -40dBm until a 1dB decrease gain was noted.
The power going to the LNA was known by measuring the probe power with the power meter, which was calibrated with its self calibration. The cable going to the power meter was also calibrated.

Noise figure measurements were measured using the noise figure meter in conjunction with the noise source. The noise source and meter where calibrated together. The source was connected to the LNA through the cable and probe. The LNA output was connected to the noise figure meter. The noise figure meter allowed insertion loss to and from the DUT to be entered to account for cable loss. Phase information could not be accounted for with this system.

The Keithly power supplies have built in voltage and current meters, but the Fluke multi meters were used to test the voltages at the probes as verification.
APPENDIX F

MULTIBAND USE

The possibility of using this design for multiband cellular use is presented here. The following plots are simulations from the schematic of this design. Input1 is optimally tuned for 860MHz to 930MHz while Input2 is tuned for 1.7GHz to 1.9GHz. The output is broadband matched across the bands.

**Figure F.1:** Gain (top) and noise figure (bottom) plots for Input1 tuned for 900MHz band.
Figure F.2: Top plot is input return loss (S11) and output return loss (S22). Bottom plot is the gain from the output to the active input ‘Input1’ tuned for 900MHz band.
Figure F.3: Gain from active input to inactive input (S12), and gain from inactive input to active input (S21). Active input is tuned for 900MHz and inactive input is tuned for 1.8GHz.

Figure F.4: Gain (top) and noise figure (bottom) plots for Input2 tuned for 1.8GHz band.
Figure F.5: Top plot is input return loss (S11) and output return loss (S22). Bottom plot is the gain from the output to the active input ‘Input2’ tuned for 1.8GHz band.

Figure F.6: Gain from active input to inactive input (S12), and gain from inactive input to active input (S21). Active input is tuned for 1.8GHz and inactive input is tuned for 900MHz.
BIBLIOGRAPHY


[9] Professor Steven C. Reising, Phone conversations and emails, February – March 2006


[18] T. Benalia and A. Monga, Several phone conversations, March, April and August, 2007

